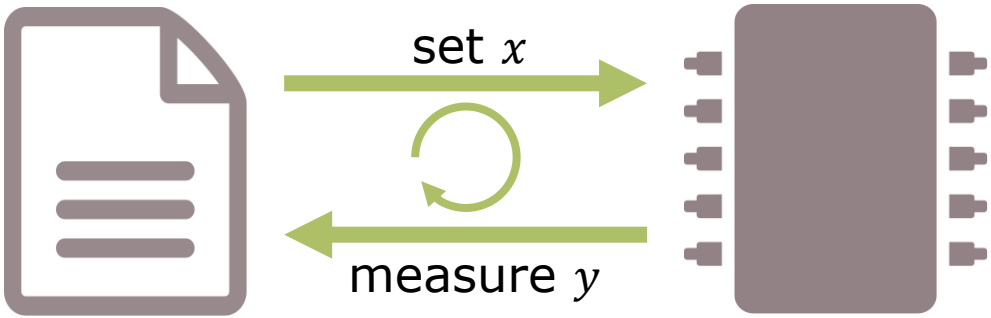
# Behavioral Modeling for SoC Simulation
## Bridging Analog and Firmware Demands

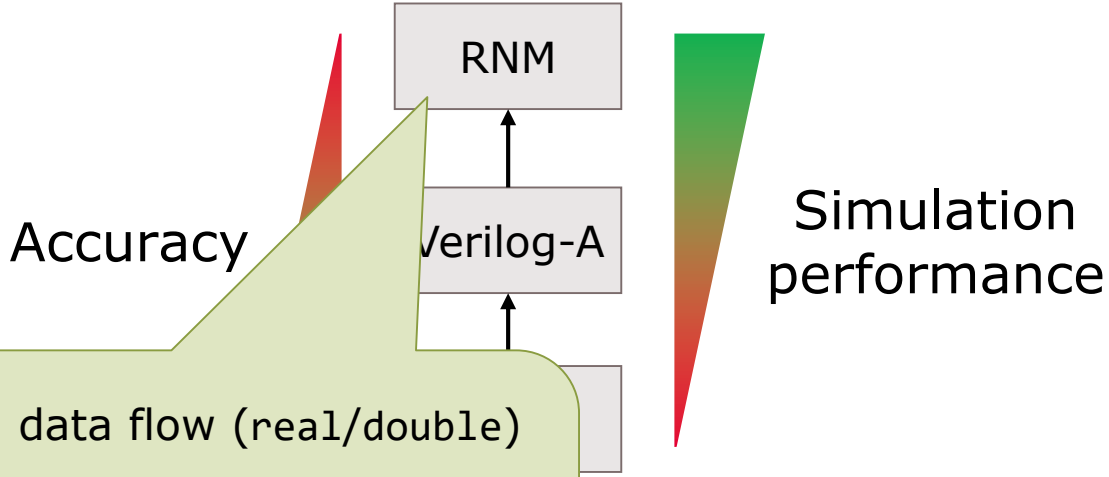
Rainer Findenig
Infineon Technologies

# System-Level Verification



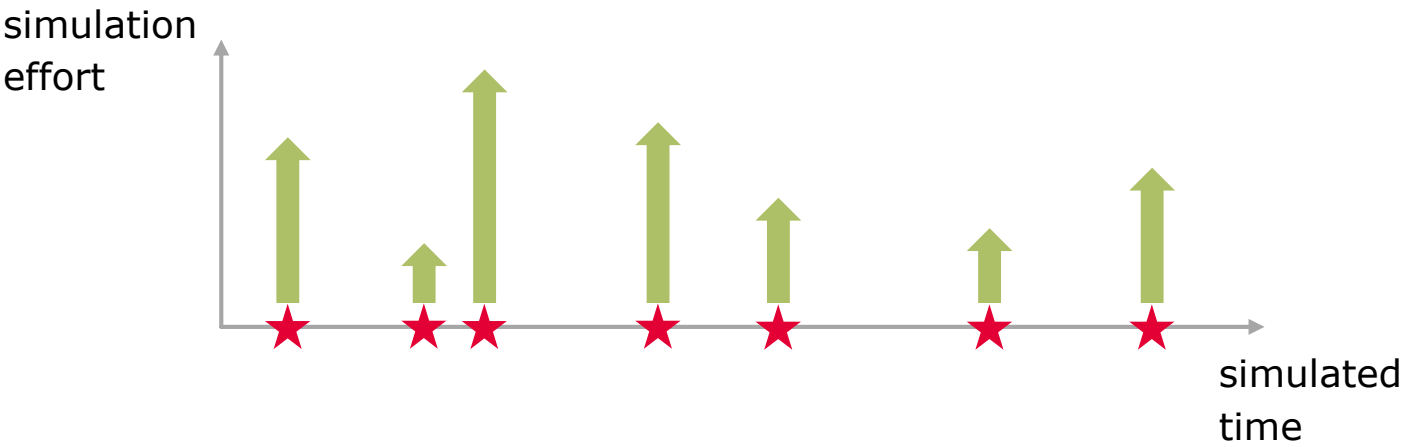

"Set $x$ to achieve optimized $y$!"

# Analog Abstractions

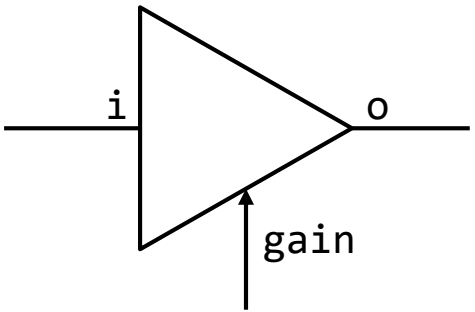



- Unidirectional data flow (`real/double`)
- Continuous value, discrete time
- No analog solver required
- Event-driven simulator

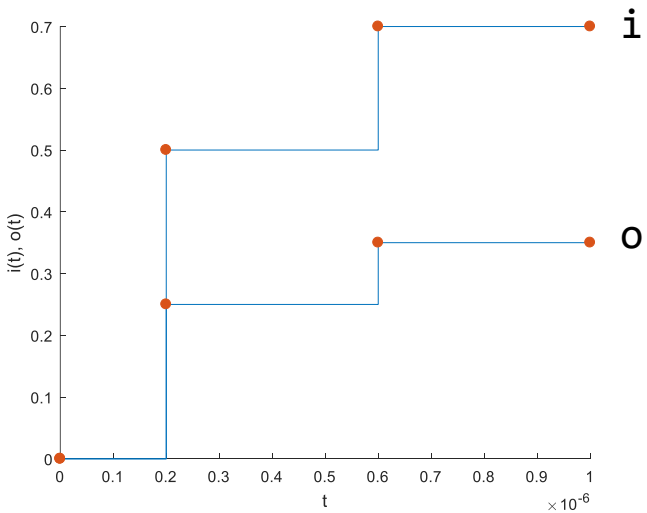
# Event-Driven Simulation



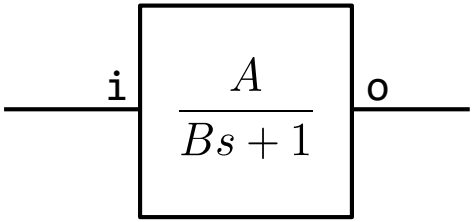
# Real-Number Modeling



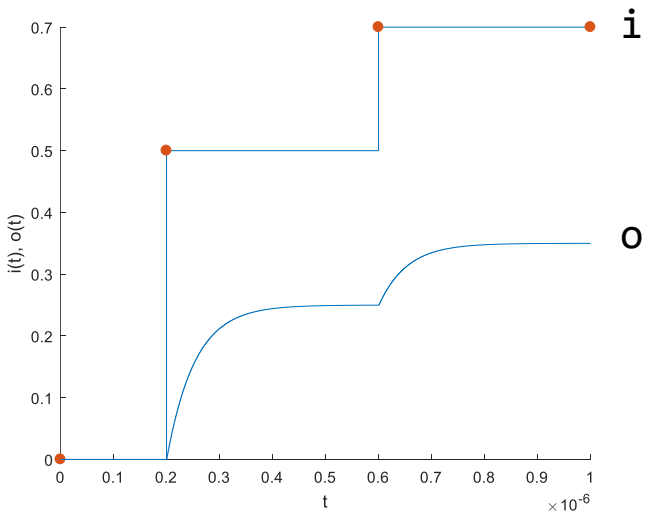

```
always @(i, gain)
    o = i * gain;
```



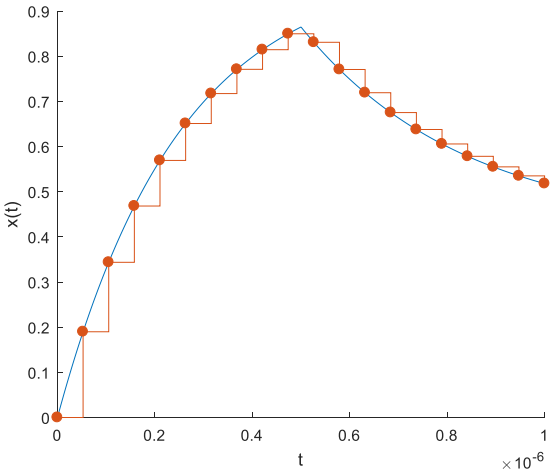
# Real-Number Modeling




?

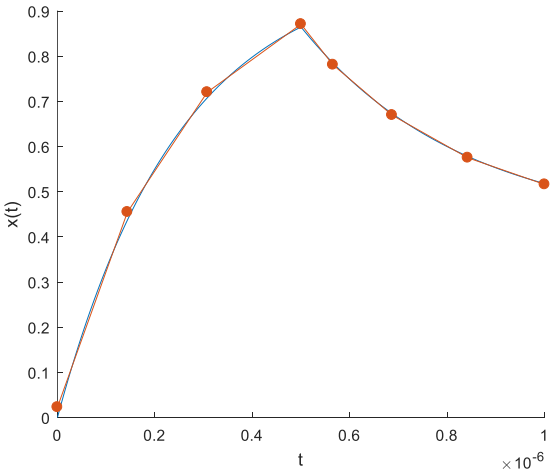


# Representing Analog Signals



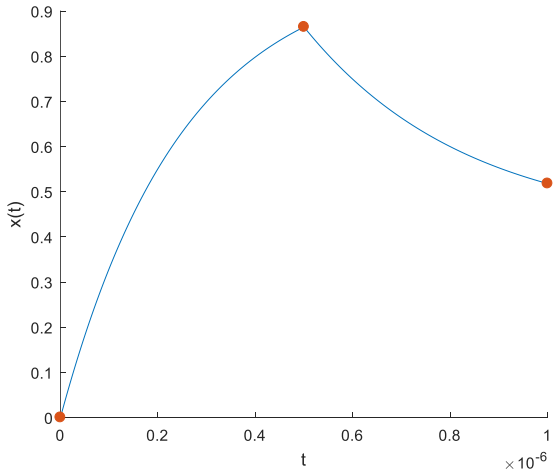

piecewise constant

$$x(t) = a$$




piecewise linear

$$x(t) = a + b(t - t_0)$$



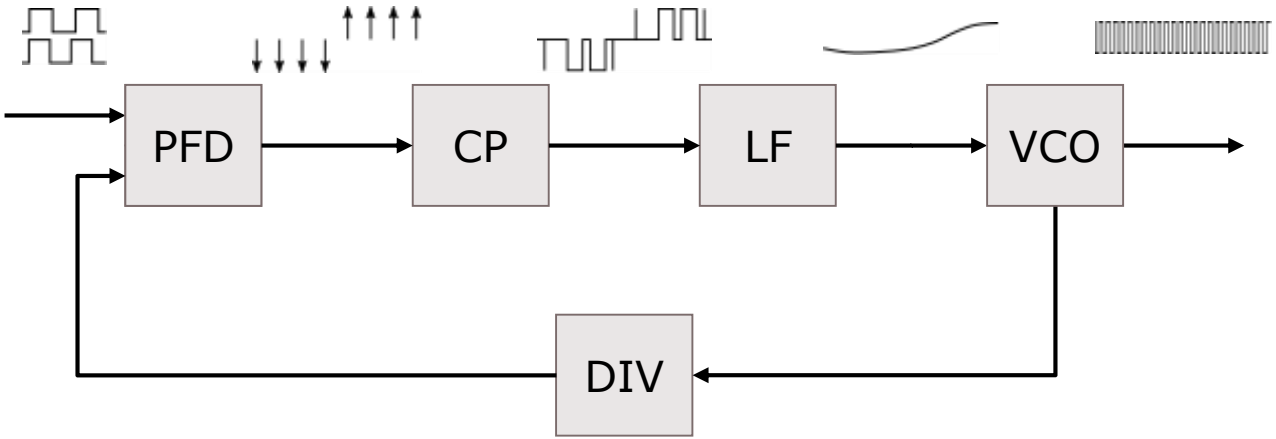

piecewise exponential

$$x(t) = a_0 + \sum_i a_i e^{-p_i(t-t_0)}$$

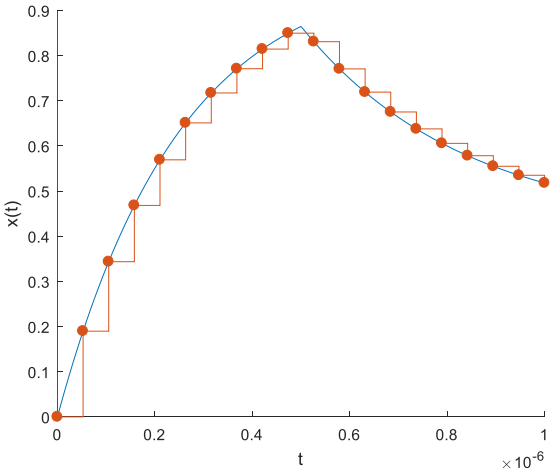

B. C. Lim, J. E. Jang, J. Mao, J. Kim, and M. Horowitz, "Digital Analog Design: Enabling Mixed-Signal System Validation," *IEEE Design Test*, vol. 32, no. 1, pp. 44–52, Feb. 2015.

J. E. Jang, M. J. Park, D. Lee, and J. Kim, "True event-driven simulation of analog/mixed-signal behaviors in SystemVerilog: A decision-feedback equalizing (DFE) receiver example," in *Proceedings of the IEEE 2012 Custom Integrated Circuits Conference*, 2012, pp. 1–4.

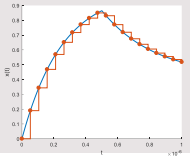
# Modeling an Analog PLL

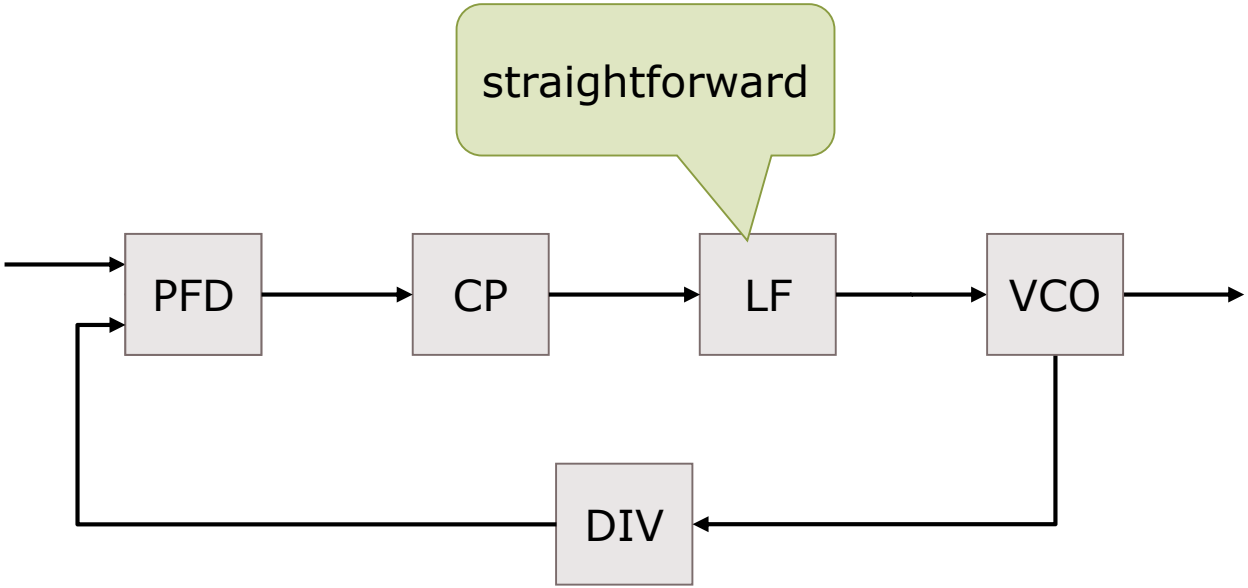


# Piecewise Constant

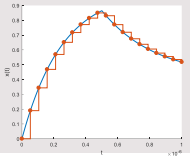


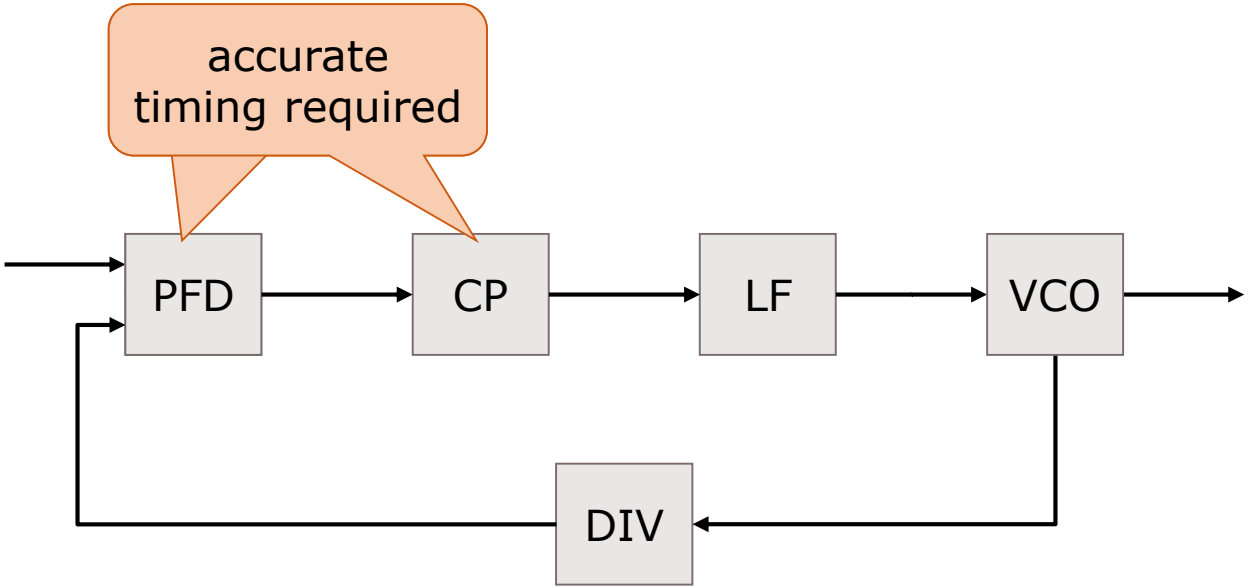
# Piecewise Constant



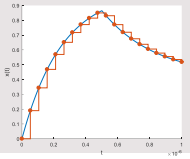


# Piecewise Constant

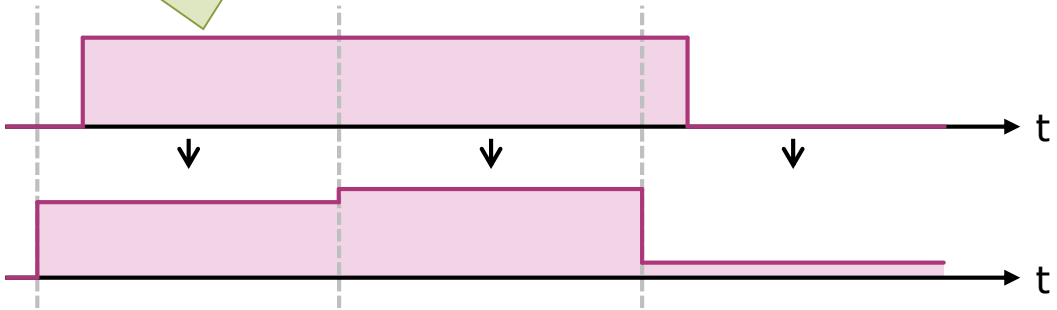




# Piecewise Constant

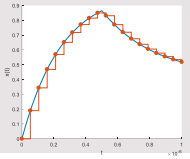


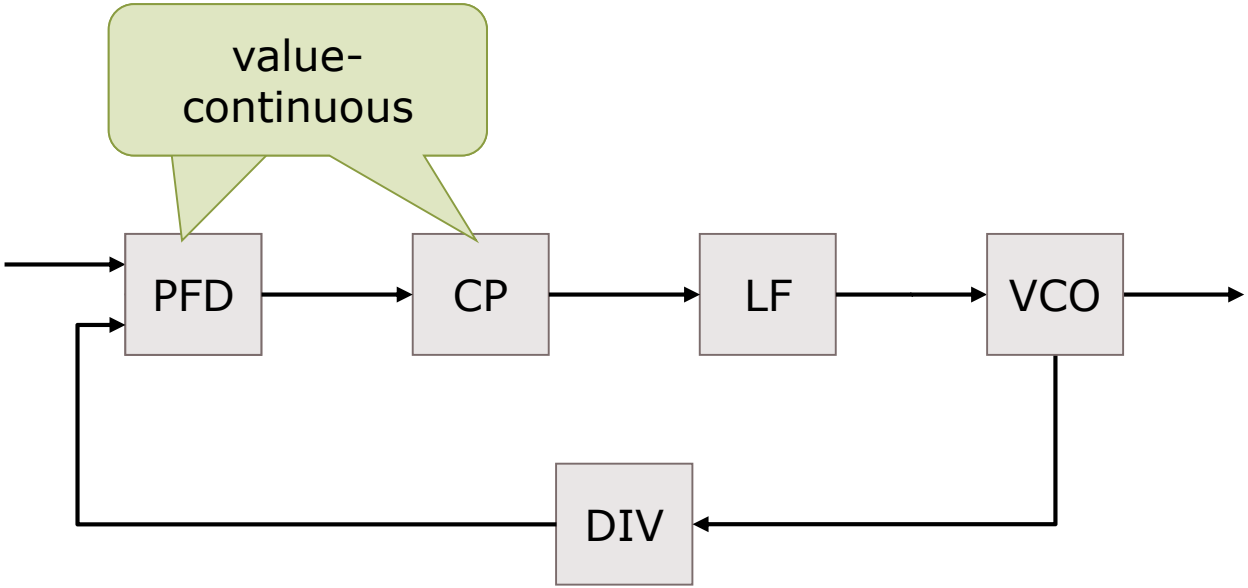
time-continuous/value-discrete
transformed to
time-discrete/value-continuous



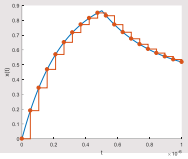

M. H. Perrott, "Fast and accurate behavioral simulation of fractional-N frequency synthesizers and other PLL/DLL circuits," in *Proceedings 2002 Design Automation Conference*, 2002, pp. 498–503.

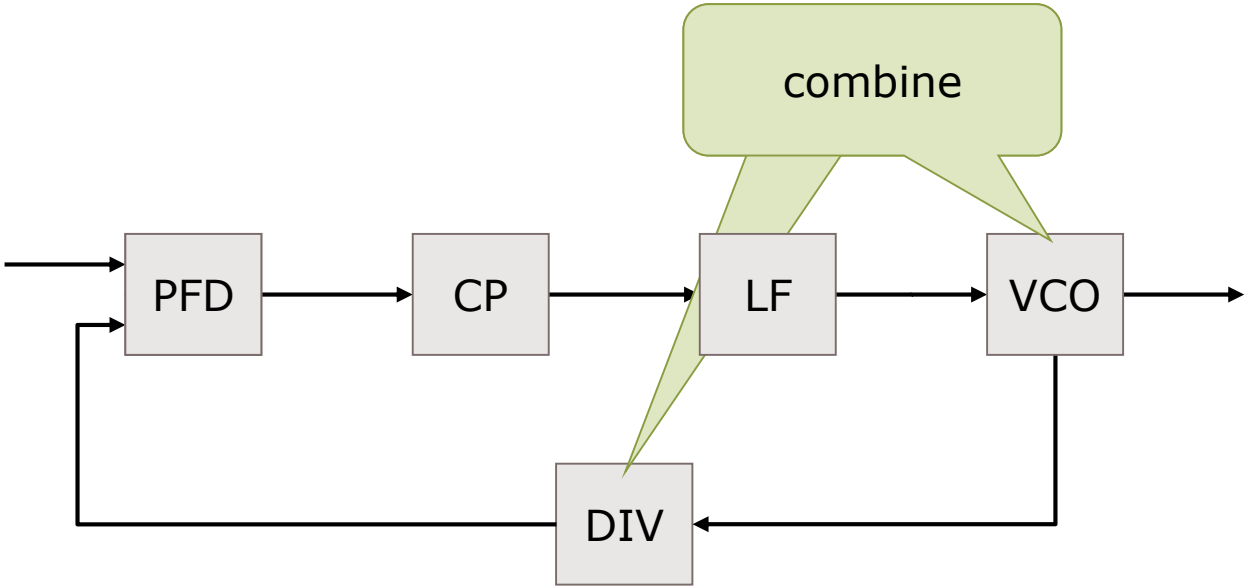
# Piecewise Constant



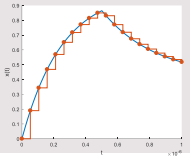


# Piecewise Constant





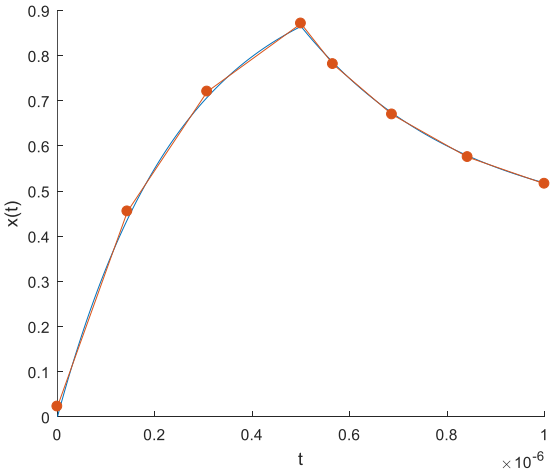
# Piecewise Constant



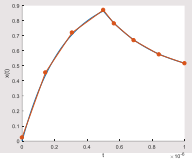
+ Easy to model
+ Structure readily obvious
+ Real-number datatypes

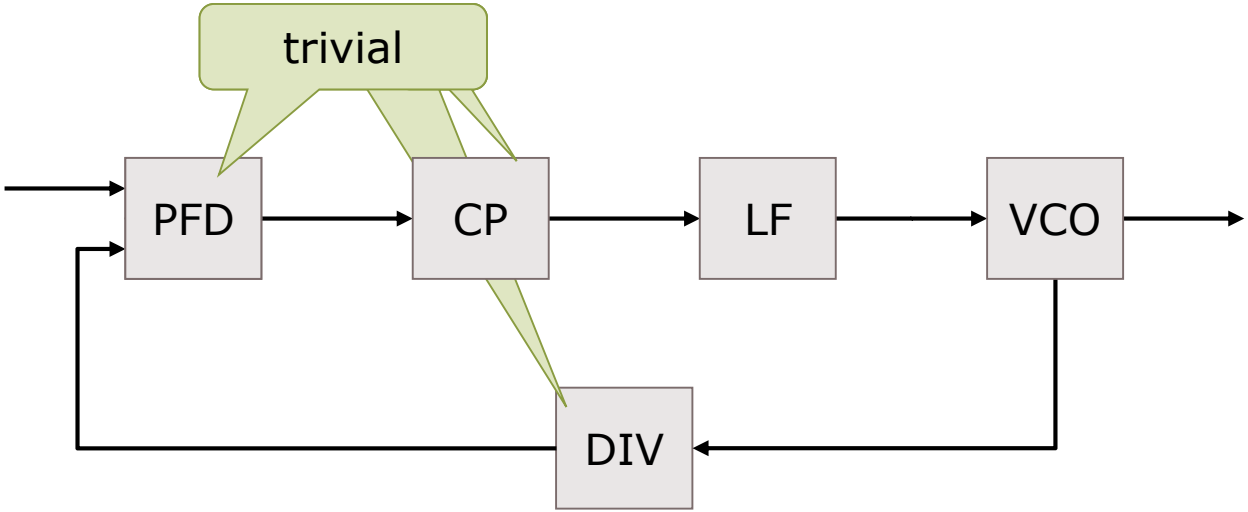
– ≥10x oversampling

# Piecewise Linear

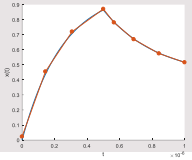


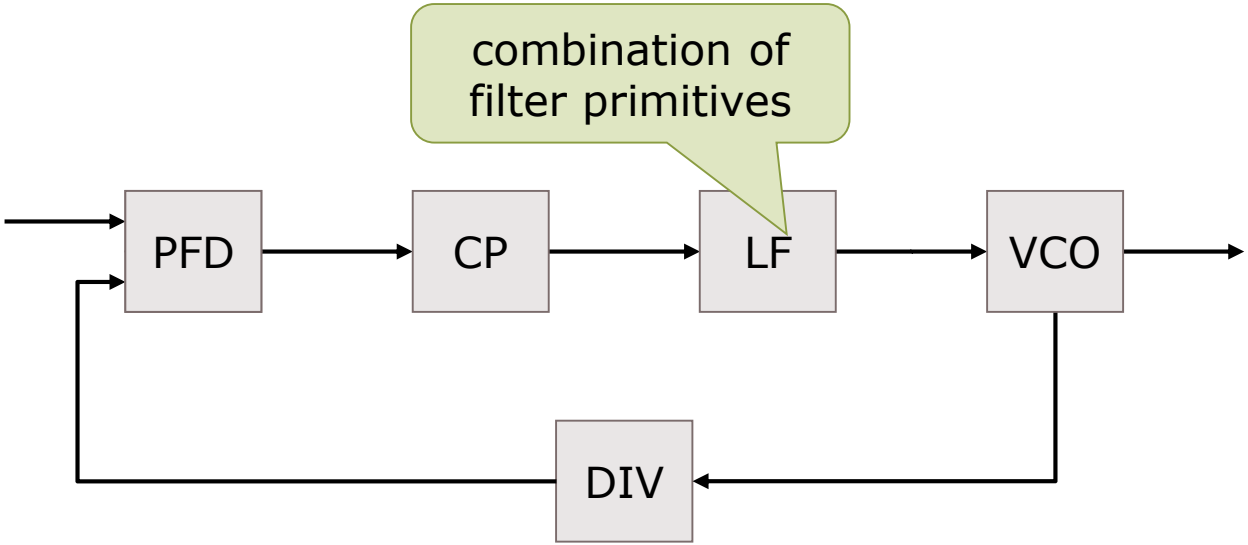
# Piecewise Linear



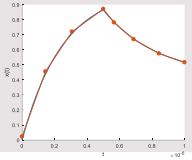


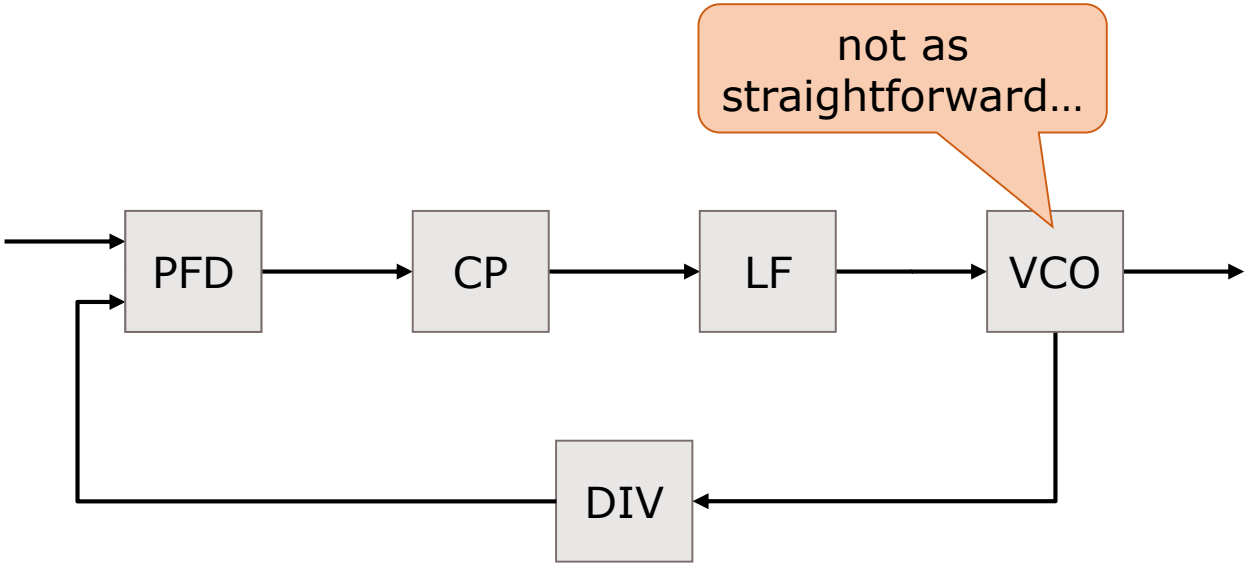
# Piecewise Linear



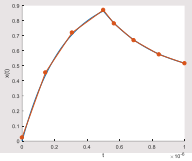


# Piecewise Linear

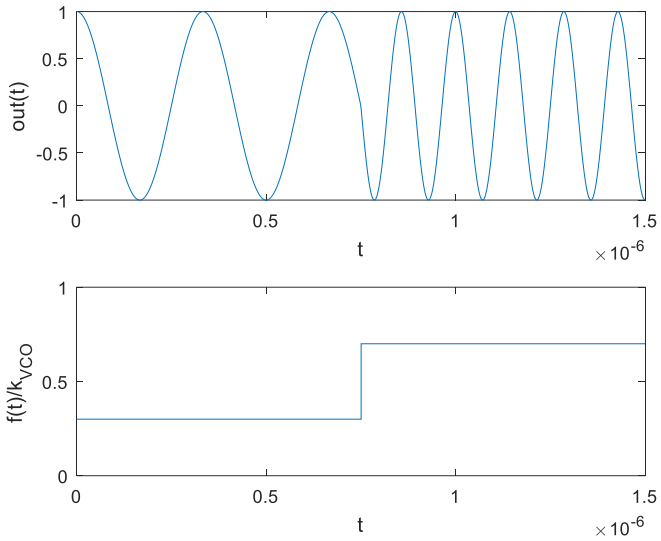




# Piecewise Linear

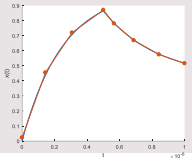


- VCO's output is highly nonlinear…

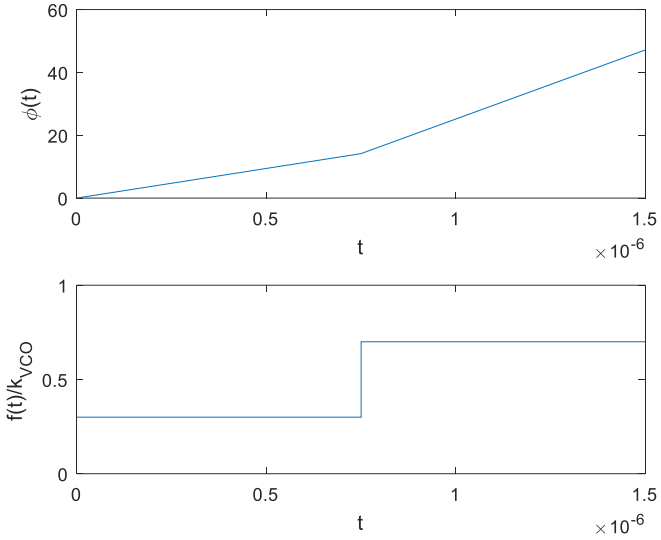



B. C. Lim, J. E. Jang, J. Mao, J. Kim and M. Horowitz, "Digital Analog Design: Enabling Mixed-Signal System Validation," *IEEE Design & Test, vol. 32*, no. 1, pp. 44-52, Feb. 2015.

# Piecewise Linear



- …but not when considering the frequency/phase domain!




B. C. Lim, J. E. Jang, J. Mao, J. Kim and M. Horowitz, "Digital Analog Design: Enabling Mixed-Signal System Validation," *IEEE Design & Test, vol. 32*, no. 1, pp. 44-52, Feb. 2015.

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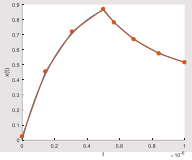
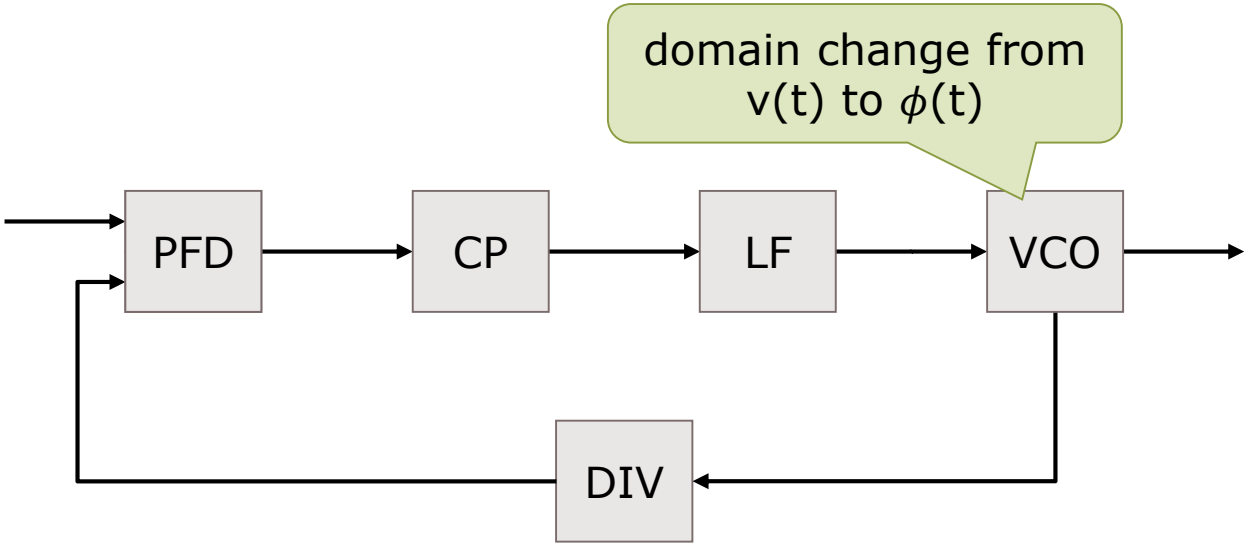
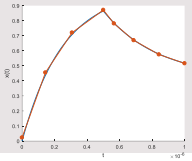




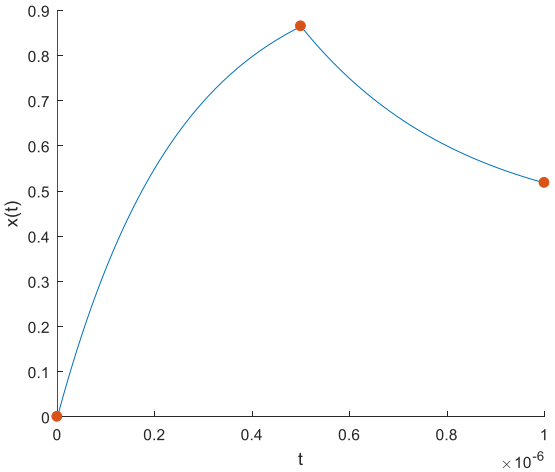
# Piecewise Linear



+ Easy to model
+ Close to original structure
+ Significantly faster

– Three-valued datatypes
– More samples than necessary

# Piecewise Exponential



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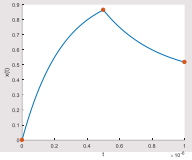
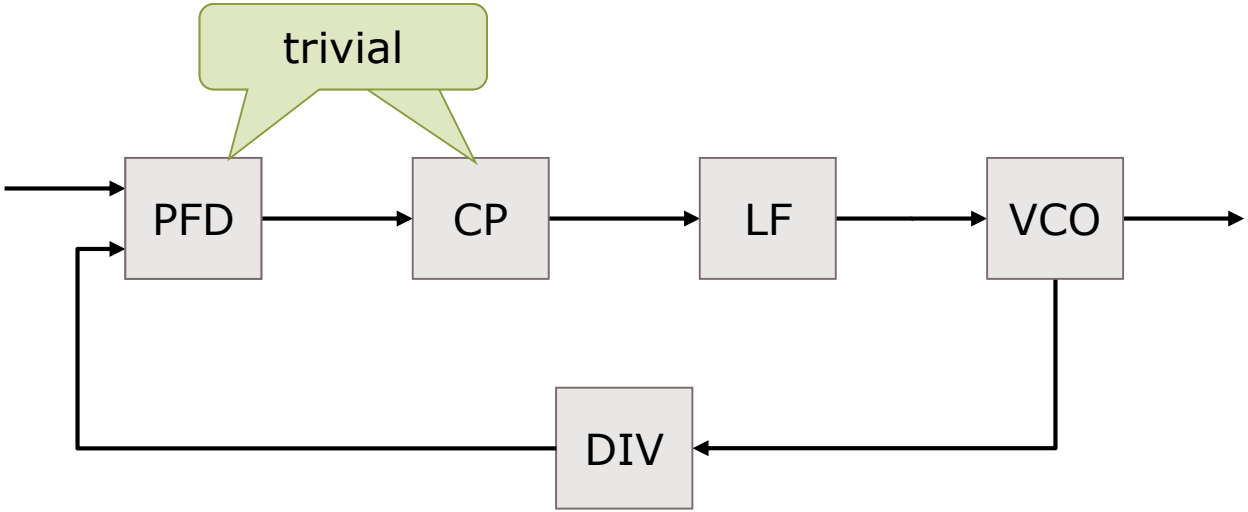
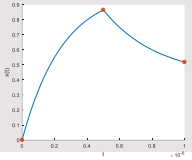
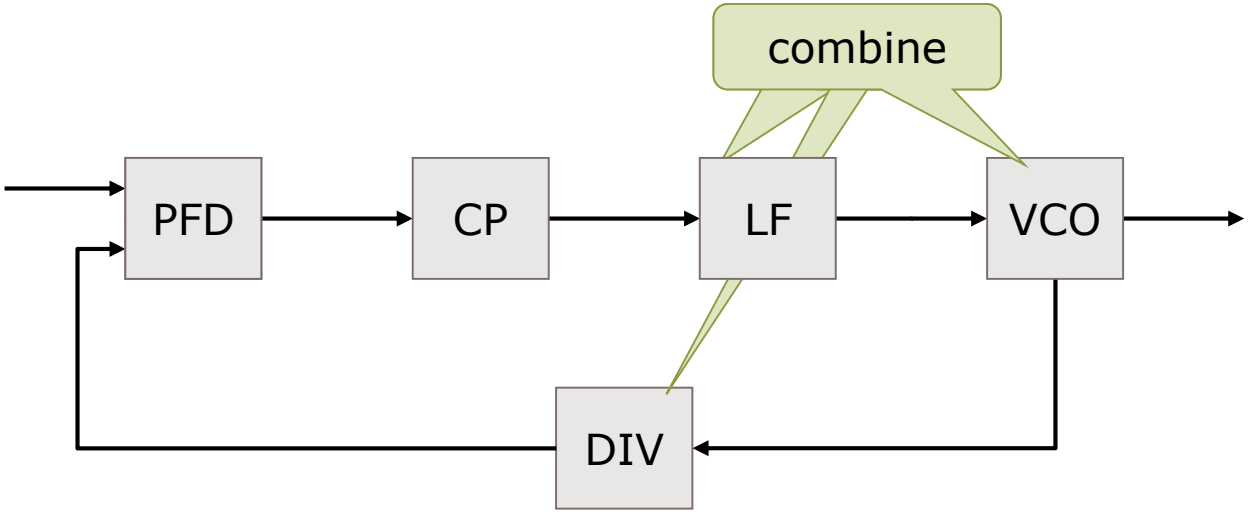


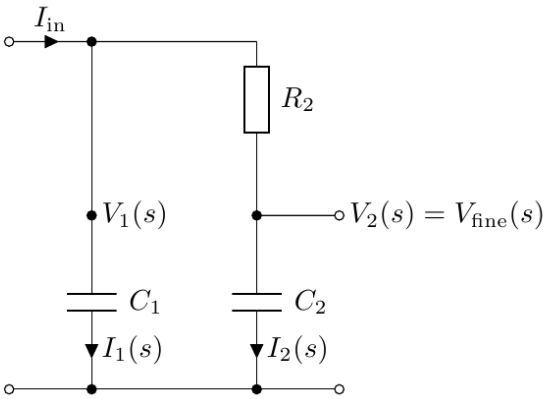


# Piecewise Exponential





# Piecewise Exponential

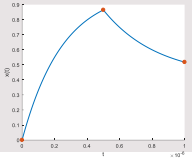


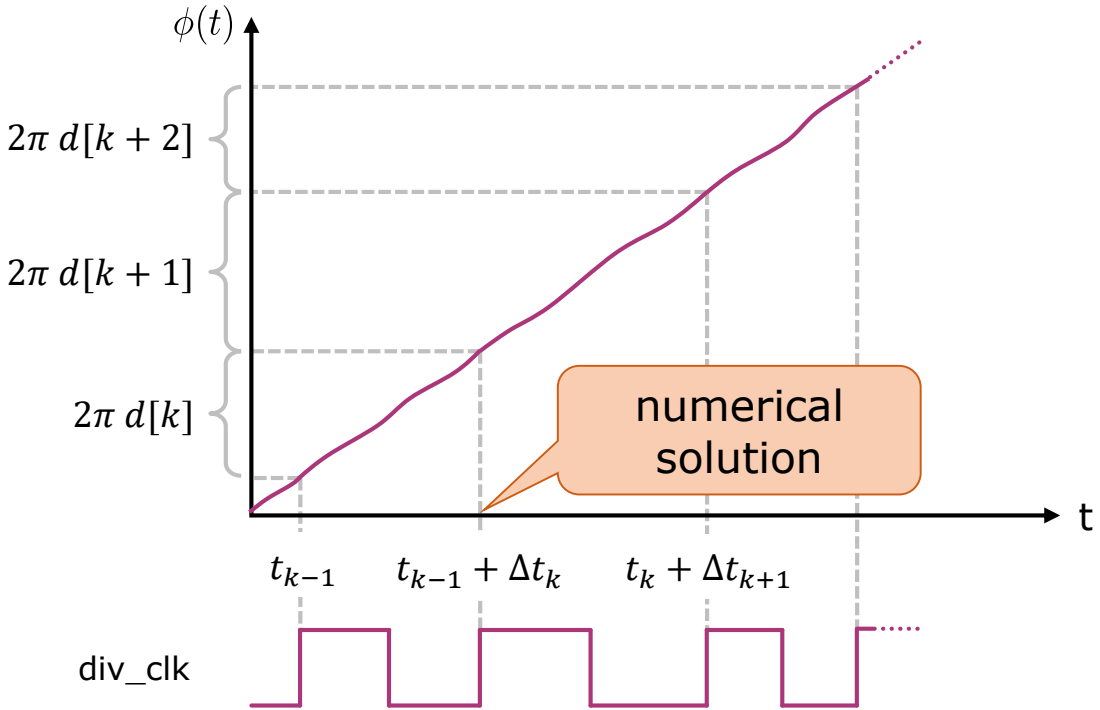

$$I_1(s) = \dots$$
$$I_2(s) = \dots$$
$$V_2(s) = \dots = V_{\text{fine}}$$
$$I_{\text{in}}(s) = \sum_i I_i(s)$$
$$\Phi(s) = 2\pi \frac{f_0 - k_{\text{vco}} v_{\text{fine}}(0)}{s^2} + 2\pi k_{\text{vco}} \frac{V_{\text{fine}}(s)}{s} + \frac{\phi_0}{s}$$

$$\phi(t) = f\left(v_0, \phi_0, i_{\text{in}}, f_0, k_{\text{vco}}, t\right)$$

M. V. Paemel, “Analysis of a charge-pump PLL: a new model,” *IEEE Transactions on Communications*, vol. 42, no. 7, pp. 2490–2498, Jul. 1994.

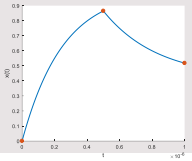
# Piecewise Exponential






M. H. Perrott, M. D. Trott, and C. G. Sodini, “A modeling approach for Σ-Δ fractional-N frequency synthesizers allowing straightforward noise analysis,” *IEEE Journal of Solid-State Circuits*, vol. 37, no. 8, pp. 1028–1038, Aug. 2002.

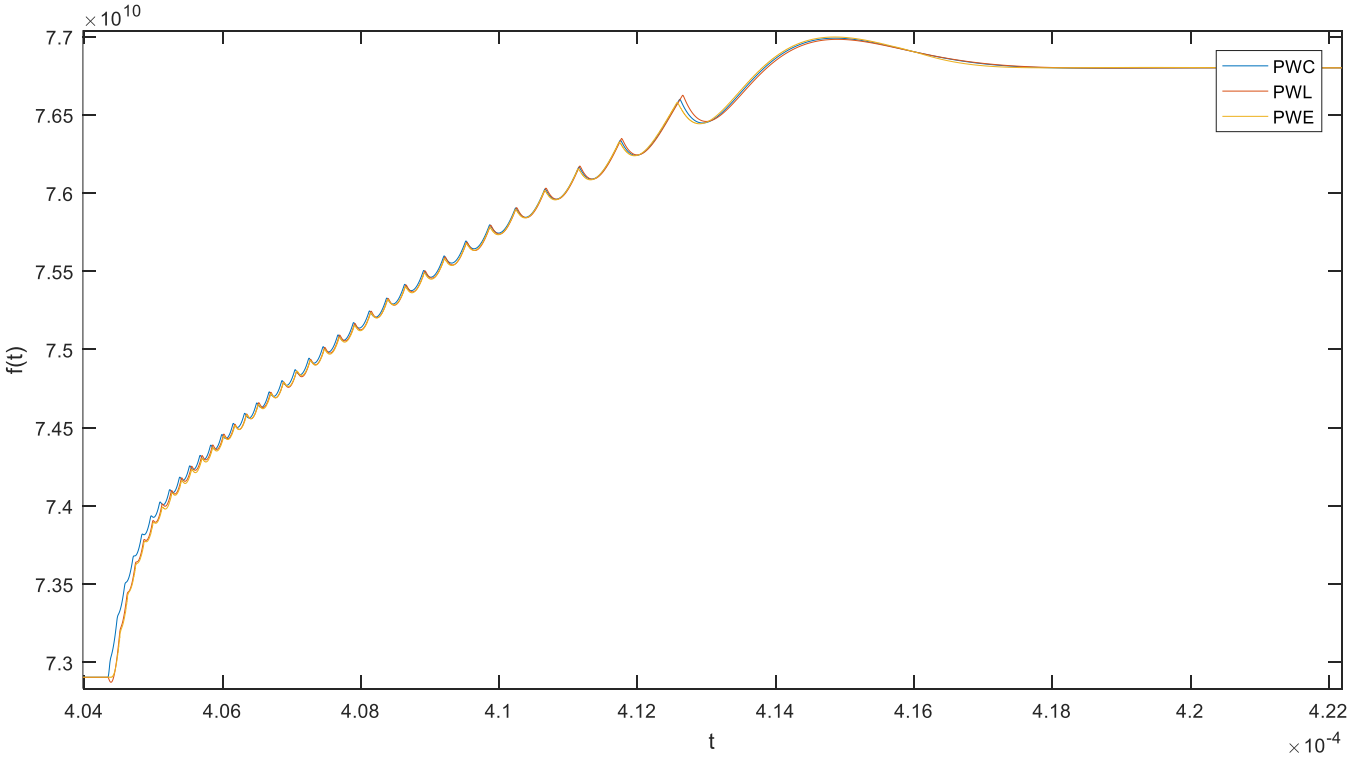
# Piecewise Exponential



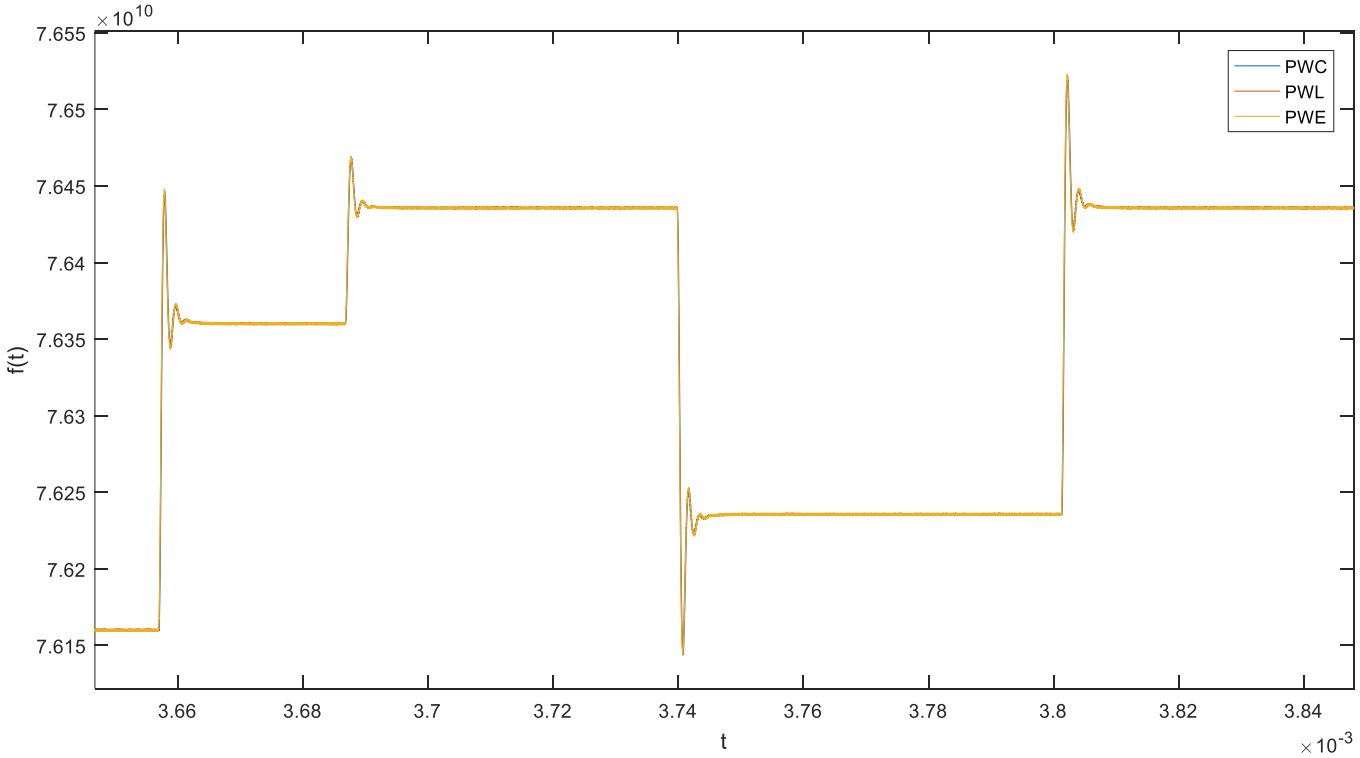
+ Minimal number of samples
+ Accurate (no approximation in LF)
+ Even faster

– Many-valued datatypes
– Equation set needs to be solved
– Numerical solution
– Loop filter and VCO not separable

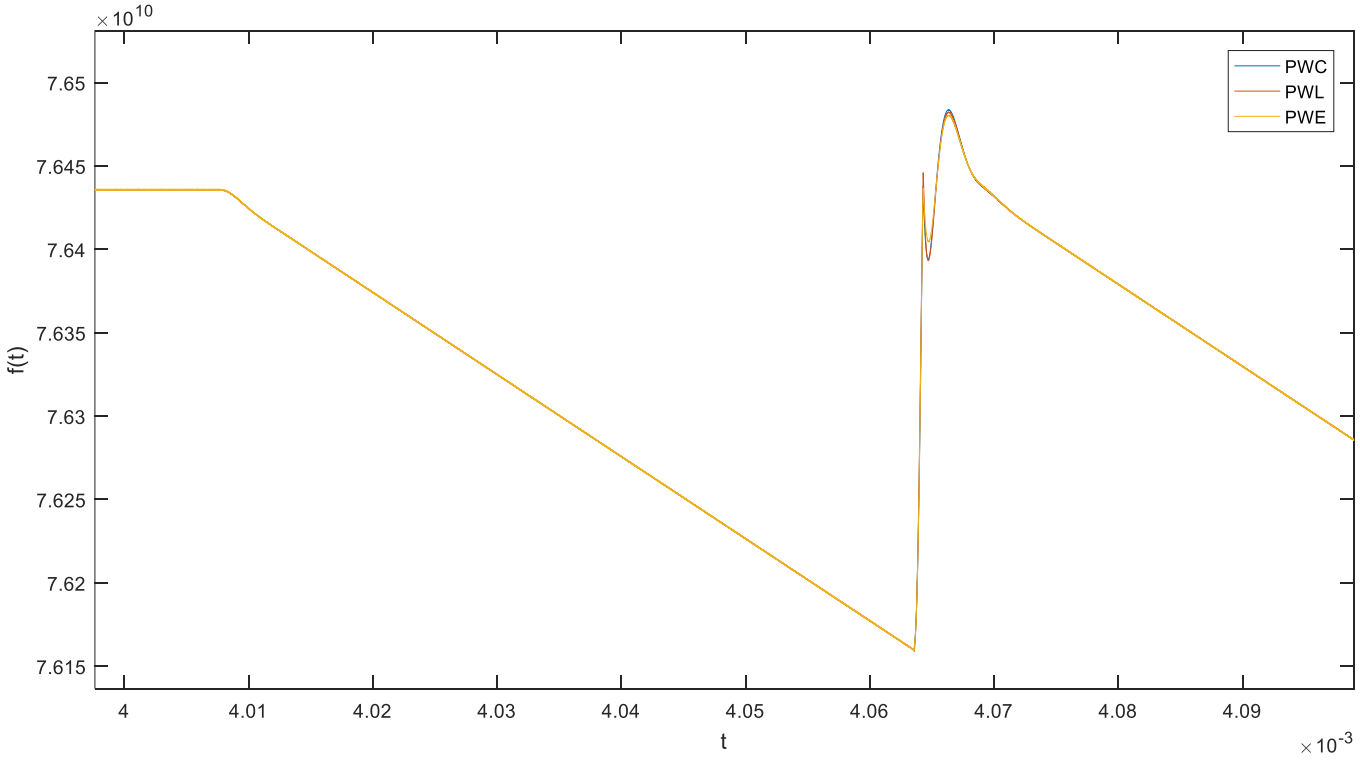
# Summary



# Summary

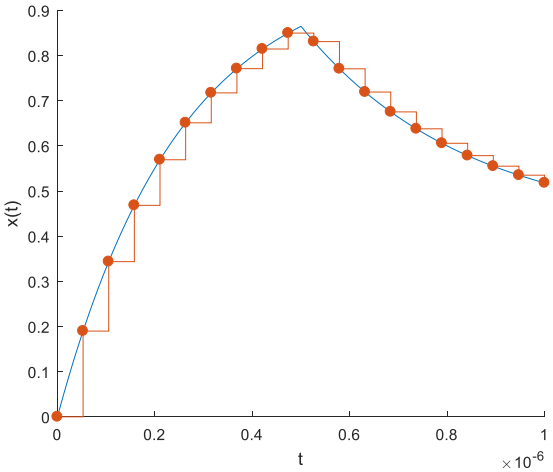


# Summary

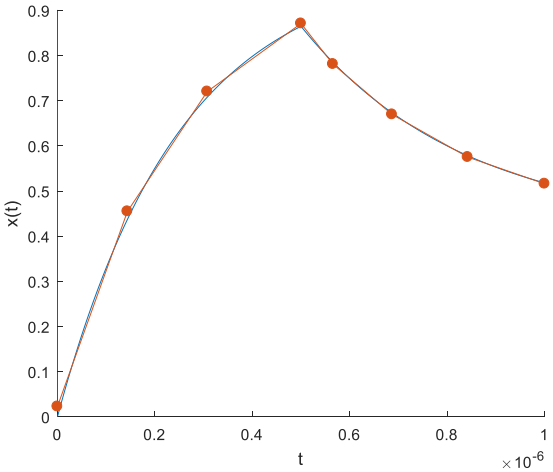


# Summary

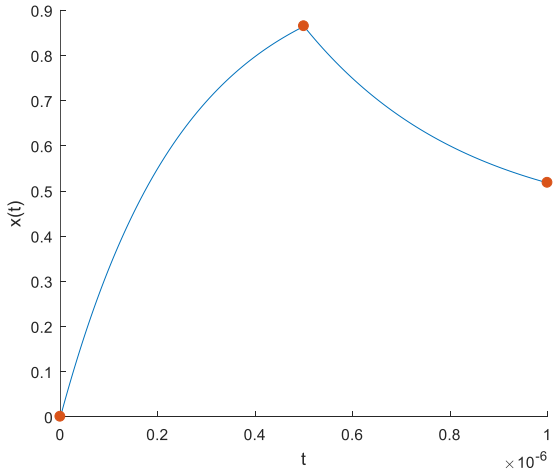
complex data type:
more information, fewer events




piecewise constant




piecewise linear

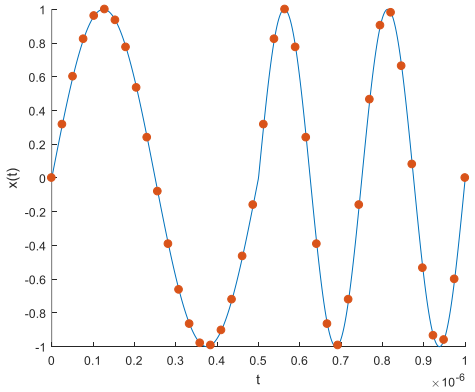


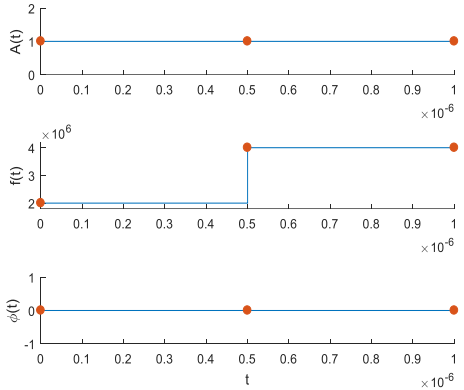

piecewise exponential

calculation complexity vs.
number of events

# Outlook

- Similar results achieved for a switch-mode power supply system
  - Digital IC + external analog components
- Representing continuous-wave signals




- Mapping functional models to FPGA/GPU

Part of your life. Part of tomorrow.

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