System Level Modelling for Mixed-Signal SoC

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Abstract— In this paper, we present a design methodology based on a multi-simulator approach instead of using co-simulation. This is targeting the design of complex SoCs, including RF and mixed signal, for system specification validation.

I. INTRODUCTION

The advances in deep sub-micronic technologies will encourage the development of a broader variety of mobile and autonomous communicating systems and devices. In the future, the amount of data exchanged between devices will continue to increase. The aim of this project is to develop a methodology and an environment to design future confident objects, able to be interfaced with various terminals and networks. These objects will include on the same SoC various communication protocols composed of the different parts: antenna, RF, analog, digital and hardware/software architectures connected with the applicative layer.

The (self-) adaptability of such systems able to operate in various environments (protocols) implies the need to approach their design in a global way. In order to address the problem of their fast and global design, we consider analog/digital co-simulation platforms on which it will be possible to model and to verify systems of a large complexity.

II. METHODOLOGY

The different parts of complex embedded systems are usually specified and designed separately by engineers working with different EDA tools. In the area of small communicating objects, it is important to take into account critical design parameters (consumption, cost, channel effects) at the system design level in order to early determine the critical parts of the design. During the system architecture exploration, one has to be provided a complete hierarchical IP-AMS model library and a unique environment supporting the use of several design flows. In the same way, the test vectors, initially applied at the system level can be reused at each design level.

The simulation time is a very important factor and can be critical. To overcome this limitation, we have introduced four-level hierarchical models (Figure 1): transistor (Spice level), structural (low level), behavioral (intermediate) and high level (ESL or Specification). To perform this, we used concurrently bottom-up and top-down approaches which allow separating significant parameters from the others. SystemC is used in order to provide a high level, C++ based and fast simulation time framework.

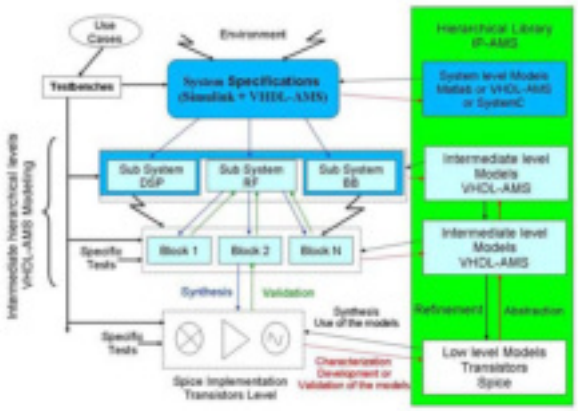

Figure 1 Methodology suggested for complex SoC development

III. CO-SIMULATION USE CASE

To demonstrate this methodology, we developed in SystemC a high level simulator of the baseband of the Bluetooth (BT) standard. This simulator can perform the complete BT baseband protocol and can verify the different protocols such as Page, Inquiry, etc.

In parallel, we developed, at different level of abstraction a complete Bluetooth transceiver using VHDL-AMS and Matlab-Simulink. One critical part of this system is the frequency generator (PLL) [1]. Therefore, we used the output of the SystemC simulator as input for the transceiver in order to validate the complete system. Different level can be used, depending on the desired simulation time.

IV. CONCLUSION

In this paper, we presented a multi-engine, multi-domain and hierarchical framework for simulating complex communicating objects at different levels of abstraction.

ACKNOWLEDGMENT)

The authors would like to thank the CIM-PACA design platform for its support

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[1] B. Nicolle, W. Tatinian, J. Oudinot & G. Jacquemod, “Hierarchical modeling of a fractional PLL”, PATMOS, Montpeiller 2006, pp. 450-457

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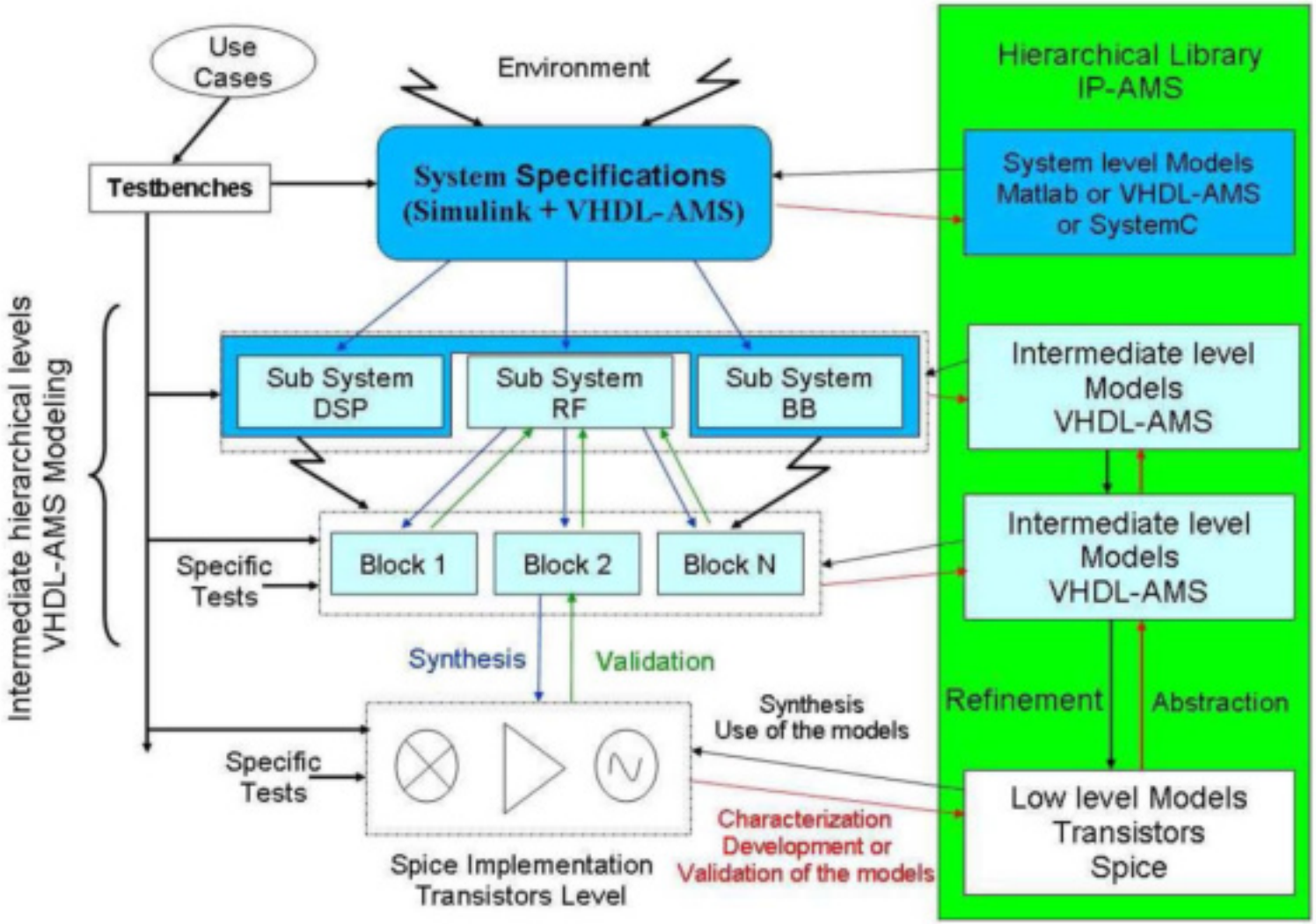
Agenda

- Introduction
- Specifications
- SystemC Modeling
- SystemC and AMS Co-Simulation
- Co-Simulation Matlab-AMS
- Conclusion

Introduction

SSCO (Small Secure Communicating Objects)
Consortium : LEAT, L2MP,
Mentor Graphics, RF Magic, NXP
Goals : Development of a methodology and a virtual platform for Specification validation of multistandard transceivers

SSCO Methodology



Application to the Bluetooth Standard

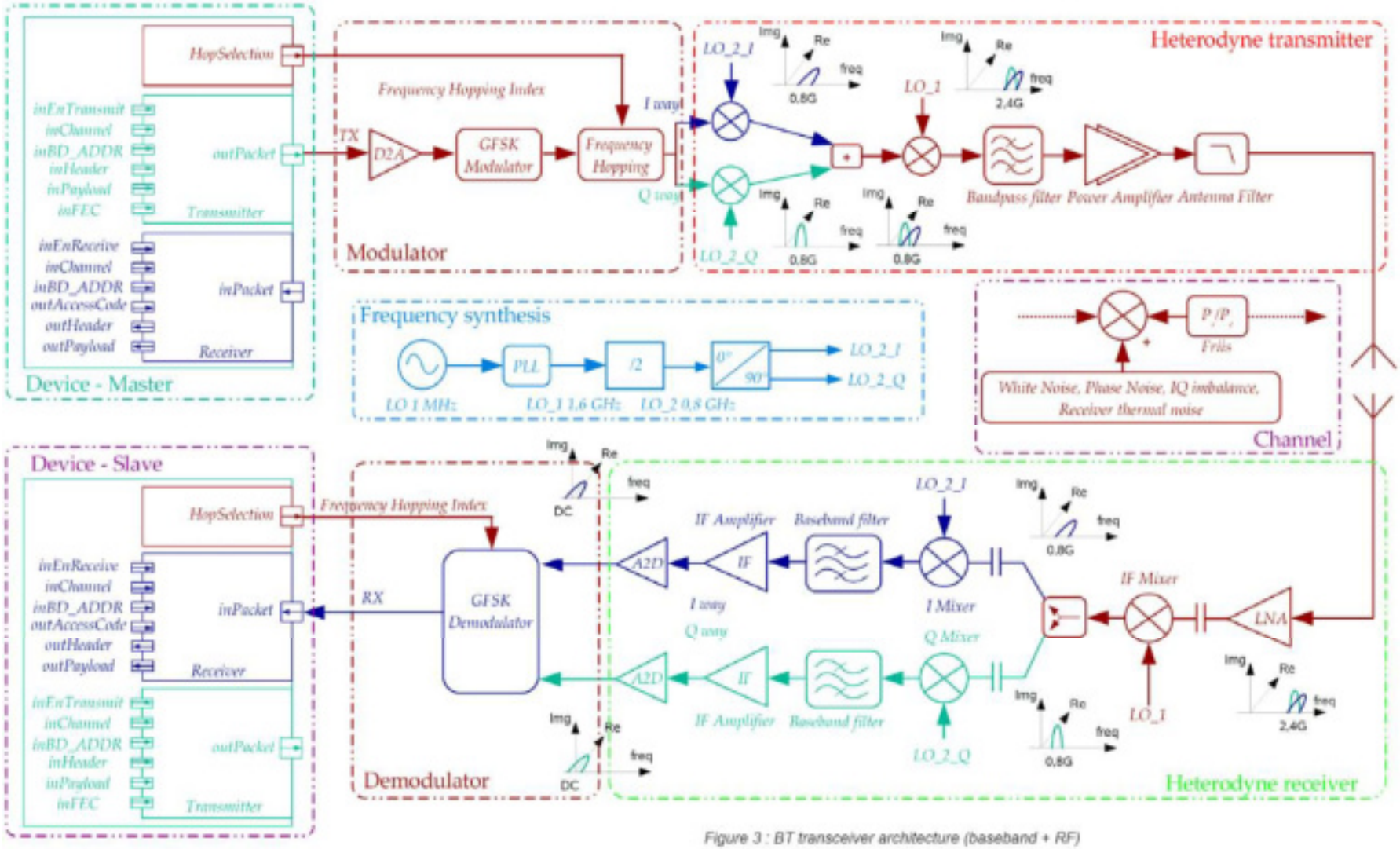
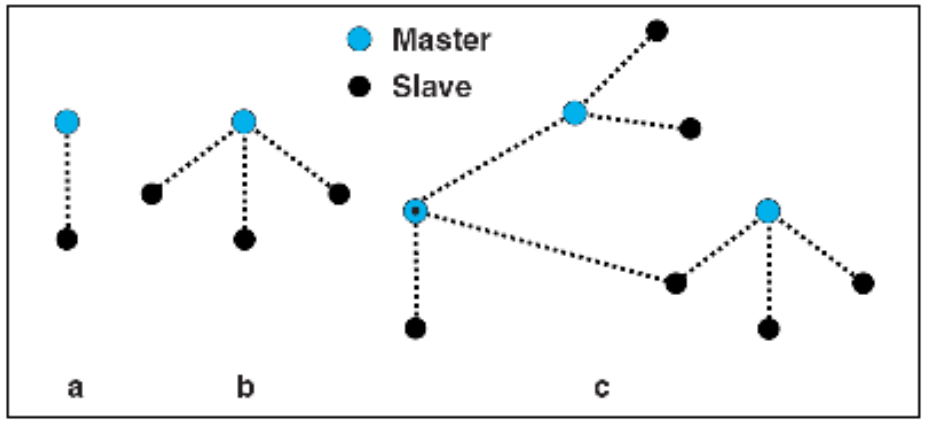


Figure 3 : BT transceiver architecture (baseband + RF)

Specifications

BT and BToUWB

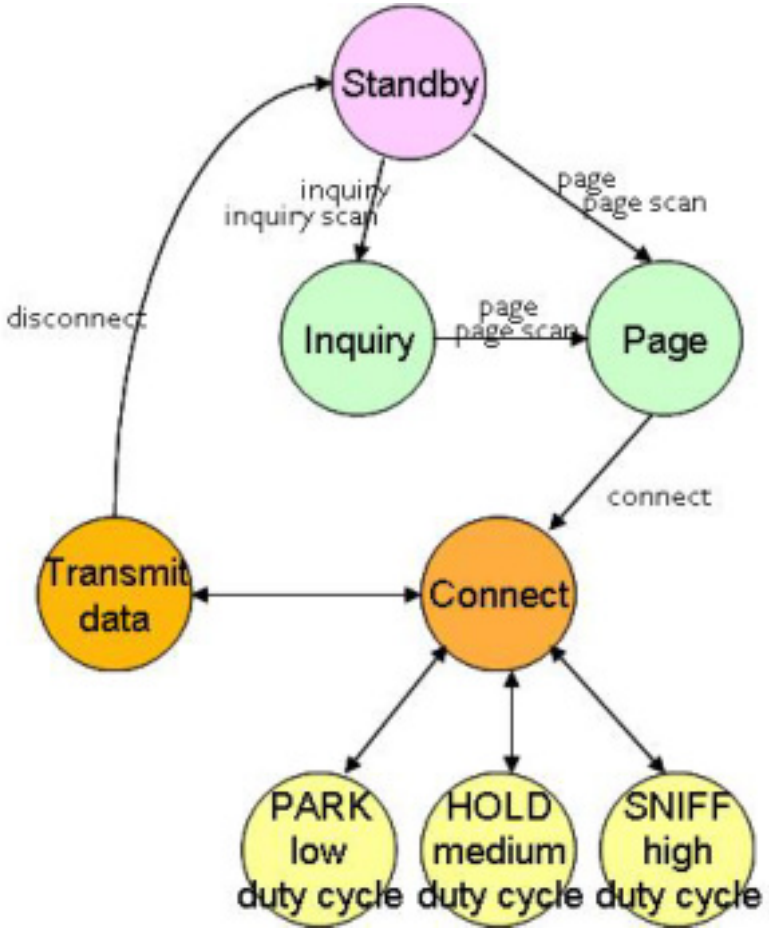
Bluetooth Specifications



- WPAN: network on short distance (from 1 up to 100 meters) using radio transmission

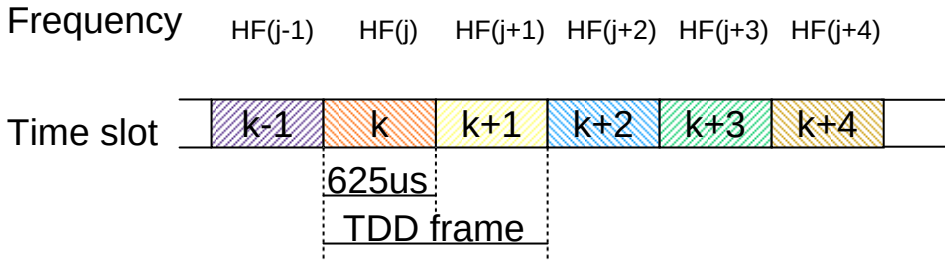
- 1 master and up to 7 slaves in one piconet
- A master can be slave of another piconet, this forms a Scatternet

Bluetooth Specifications



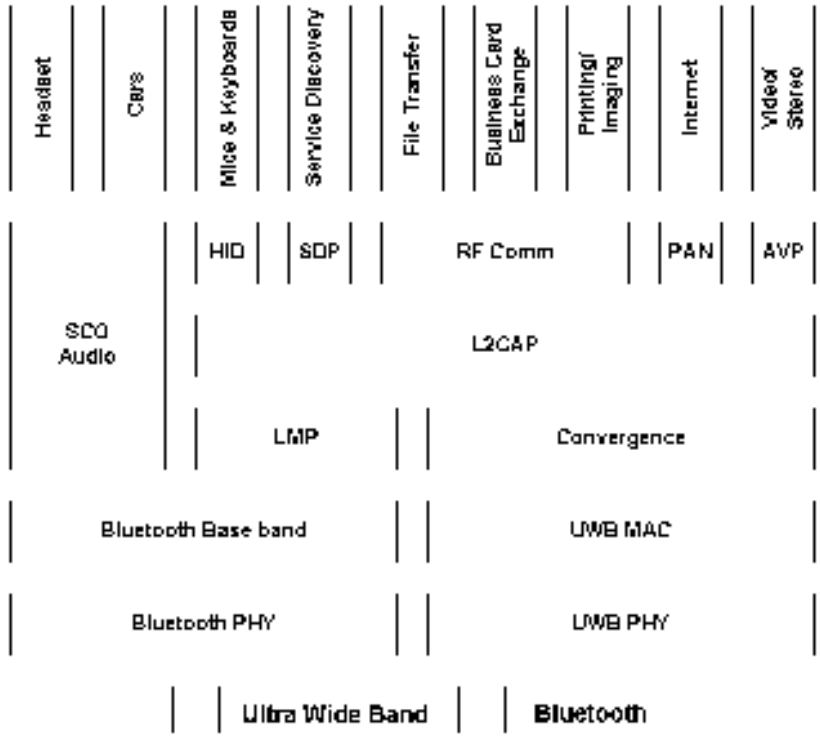
- A device exchanges different types of information depending on its state

- The channel is represented by a pseudo-random hopping sequence through 79 RF carriers
- The nominal hop rate is 1600 hops/s
- Each time slot (625us) correspond to a frequency hop



BToUWB Specifications

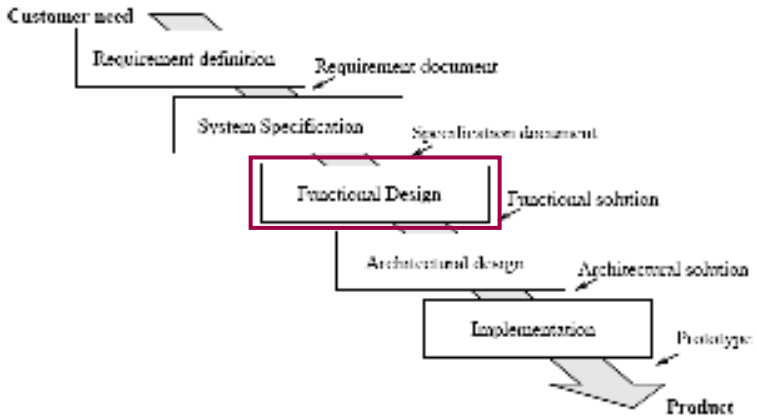
- WiMedia defines a Multiband OFDM technique to access the medium
- Data rate goes from 53.3 Mbps to 480 Mbps
- Distributed access to the medium
- Convergence layer is under specification at the Bluetooth Special interest Group (SIG)
- Main idea of BToUWB: Use the already developed and proven technology of BT to bring high data rate to the BT devices.

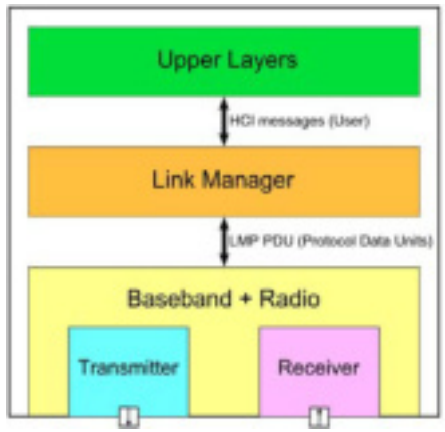


SystemC Modeling

CoDesign Methodology

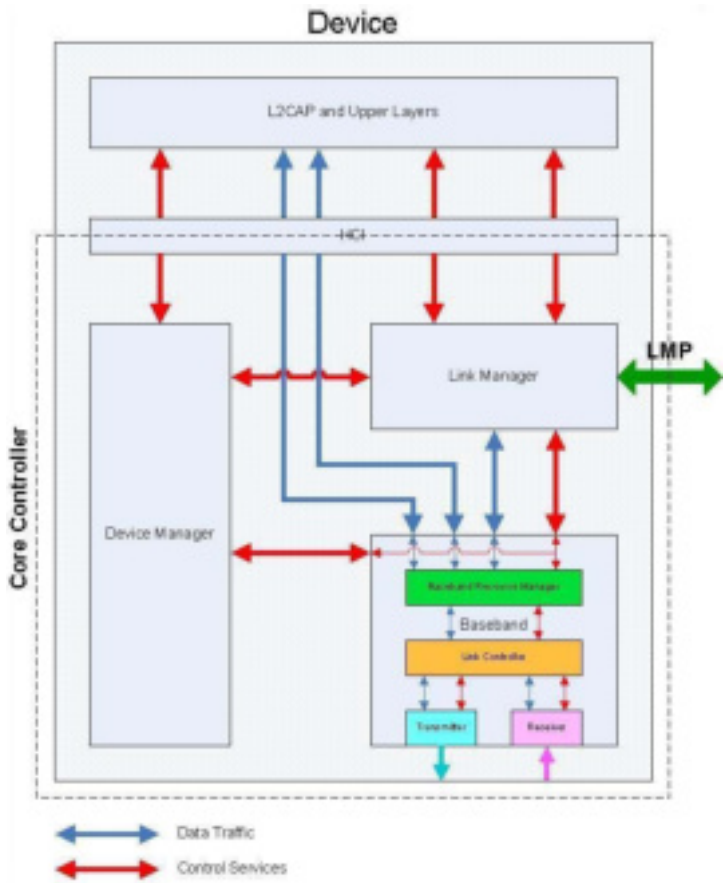
- Supports design abstraction at the RTL, behavioral and system level.
- Hardware description languages (VHDL or Verilog) lead to long simulation time and force the designer to introduce useless details about the design
- C/C++ models are profitable to describe complex IP integration and IP behaviors, in order to early confirm the design specifications
- Goal: build a functional model, which is half way between the specifications and the implementation.
- SystemC is suitable for the implementation of functional models.
- Evaluate the implementation with SystemC to validate the high-level model.





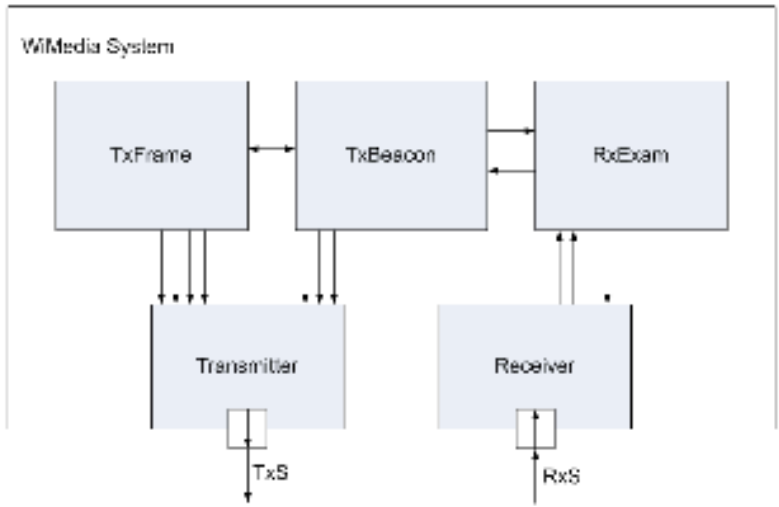
BT SystemC Model Architecture

- Description of some modules that compose a Bluetooth device:
  - L2CAP: link module between Bluetooth and WiMedia.
  - HCI: interface between the Host (above) and the Core Controller (below).
  - Device Manager: controls the general behavior of the Bluetooth Device (Inquiry/scan and Page/scan).
  - Link Manager: responsible for the creation, modification, and release of logical links.
  - Baseband: responsible for all access to the radio medium, encoding and decoding of Bluetooth packets.

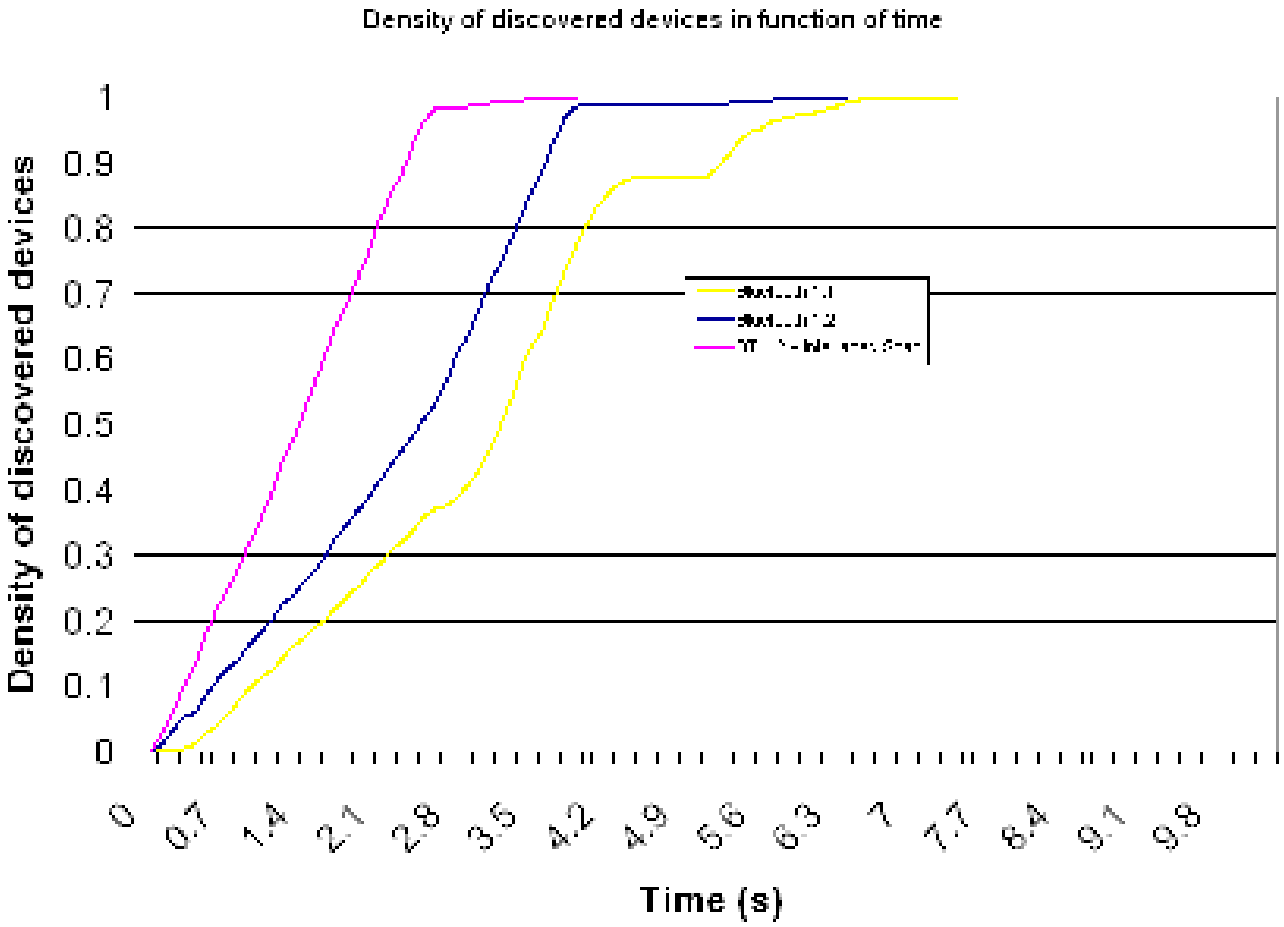


BToUWB System

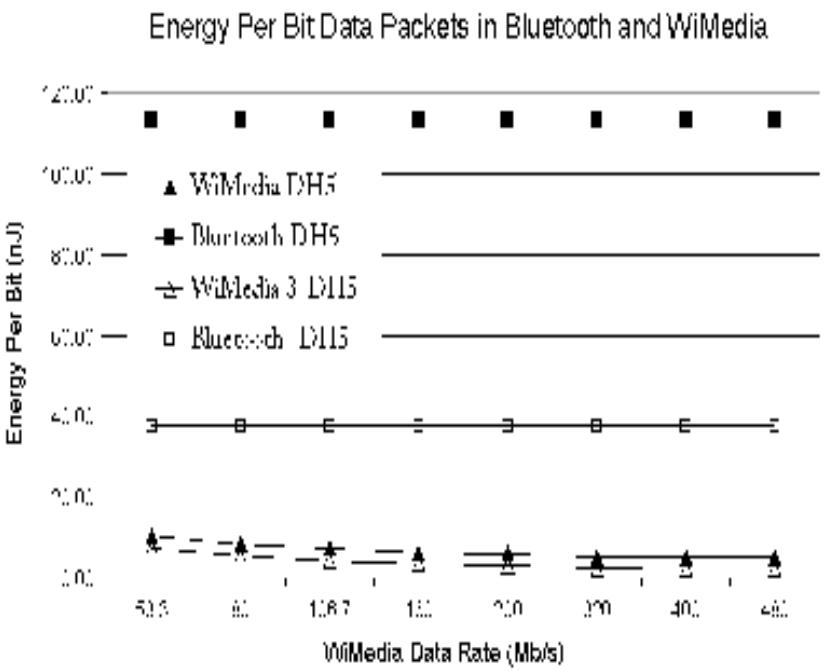
- Connection between WiMedia system and Bluetooth system is done at the L2CAP level
- Development of a high level model of the WiMedia MAC.
- Development of the convergence layer according to the standardization effort currently done in the Bluetooth SIG:
  - Algorithm development
  - Participation to the standardization effort

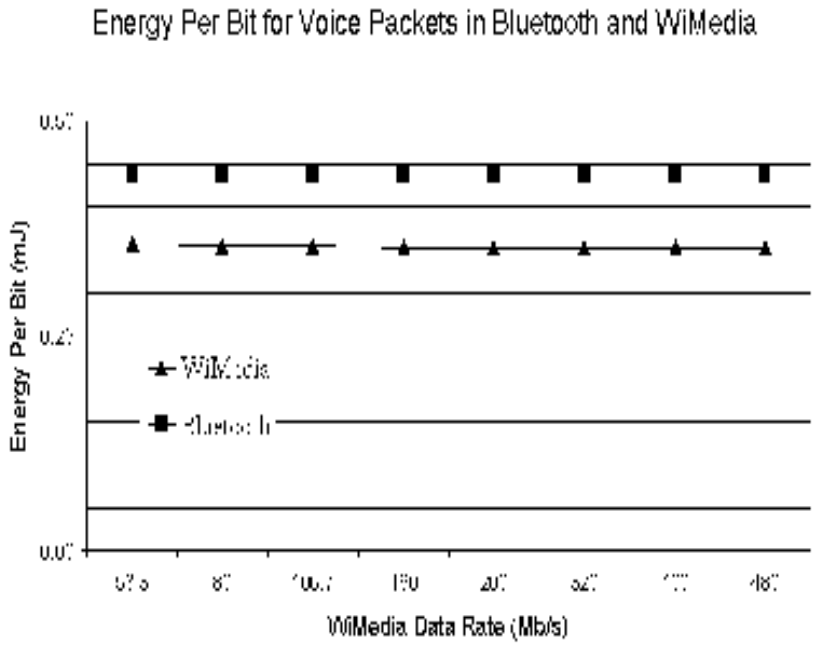


BT Model – Inquiry Response Time Results



BToUWB Results – Power Consumption





Co-Simulation between SystemC Models and AMS Models

Application to Bluetooth

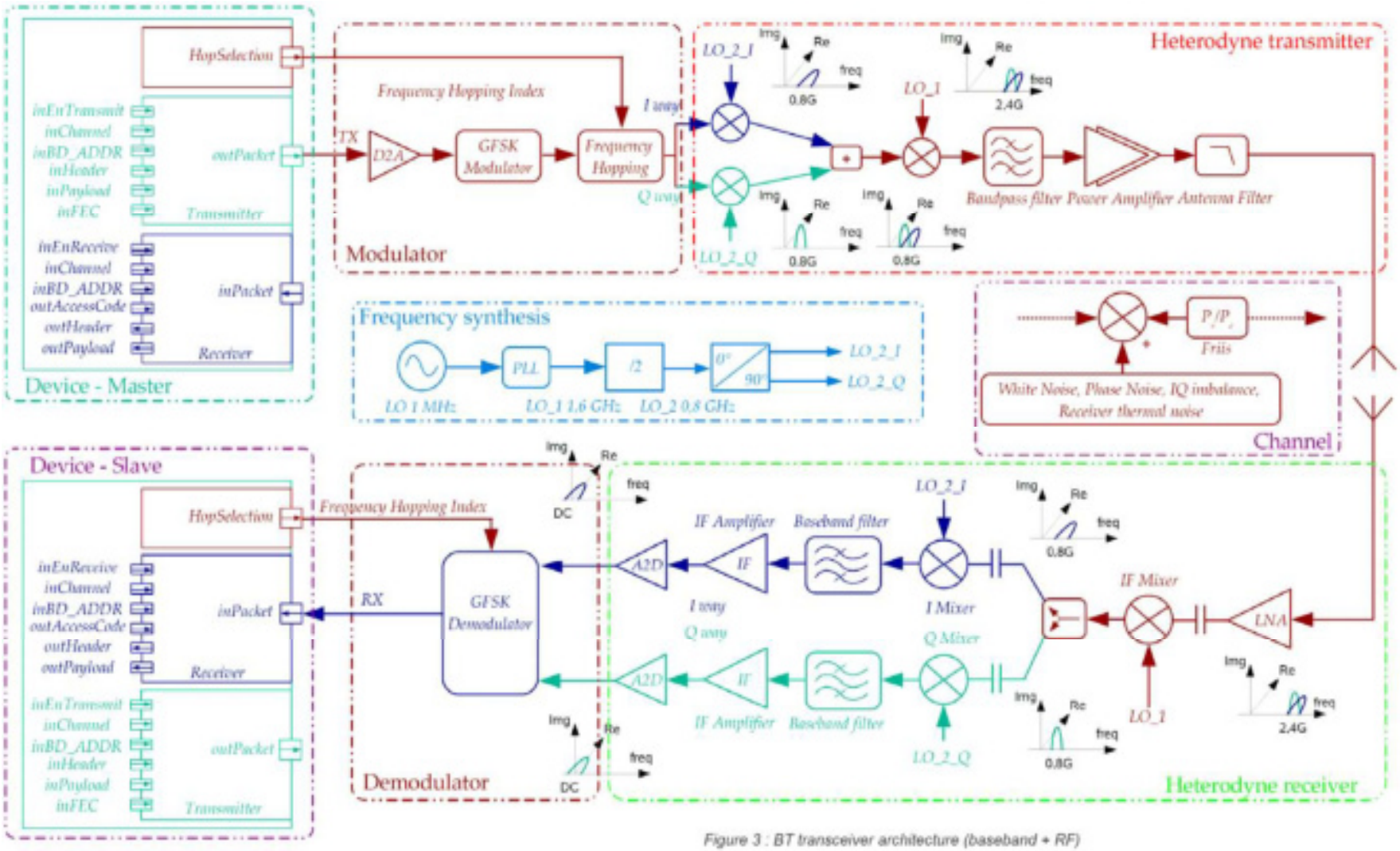
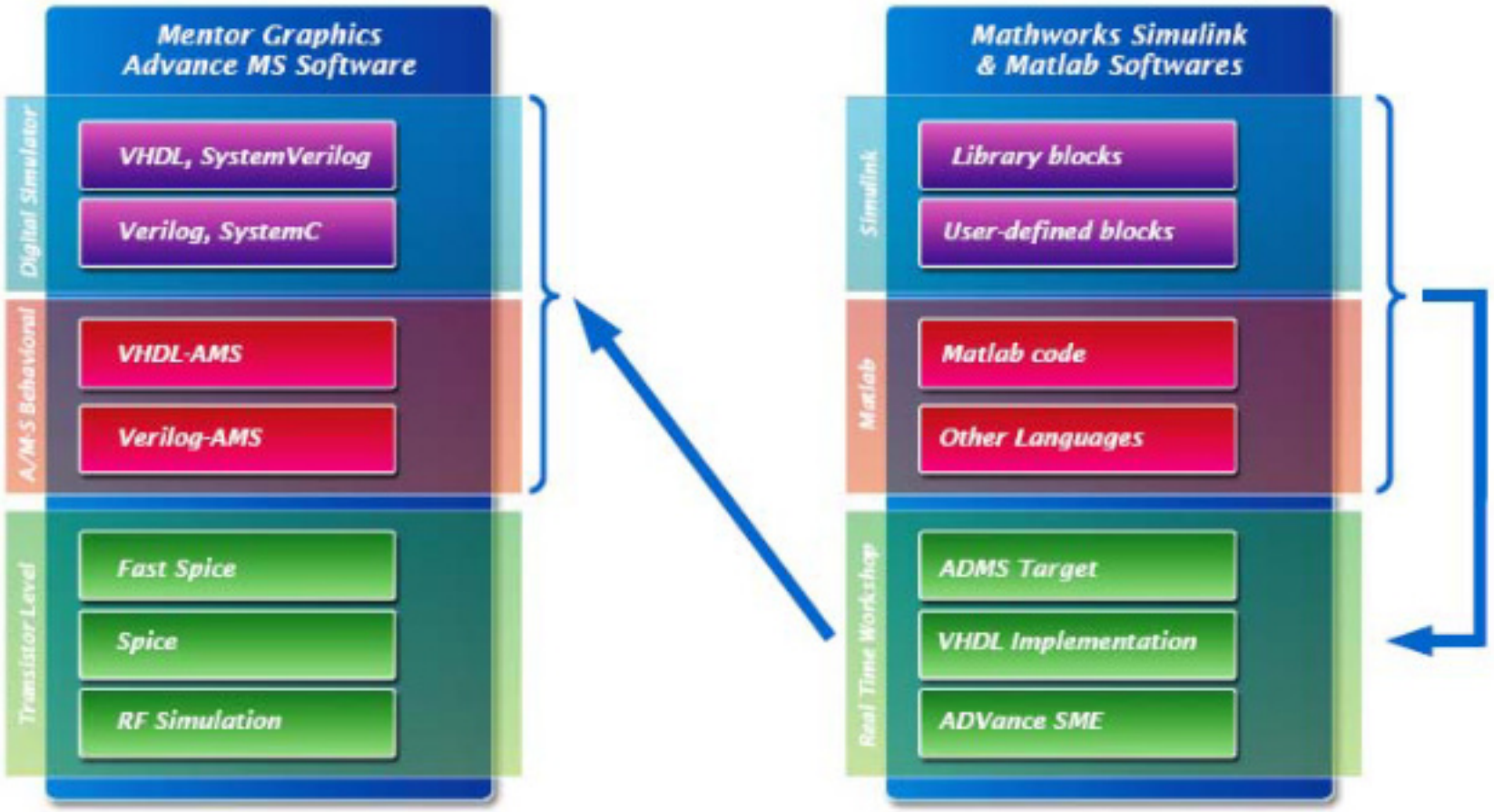


Figure 3 : BT transceiver architecture (baseband + RF)

Co-Simulation SystemC – AMS with Modelsim

- Take the SystemC Packet as input of the modulator, described in Matlab.
- Frequency hopping is driven by the SystemC model
- Under work : Steady State or circuit envelop to adapt base band reference time (10 to 100 Mbits/s) and RF time (GHz)

Co-Simulation AMS-Matlab

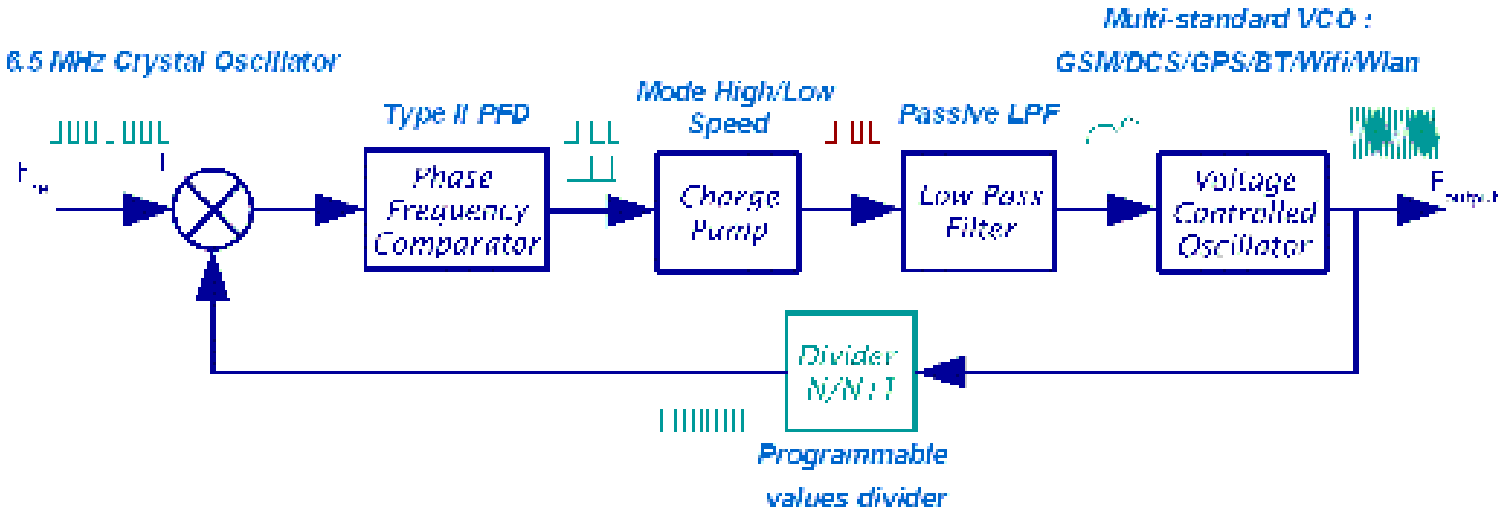


Co-Simulation Matlab-AMS

Focus on the PLL

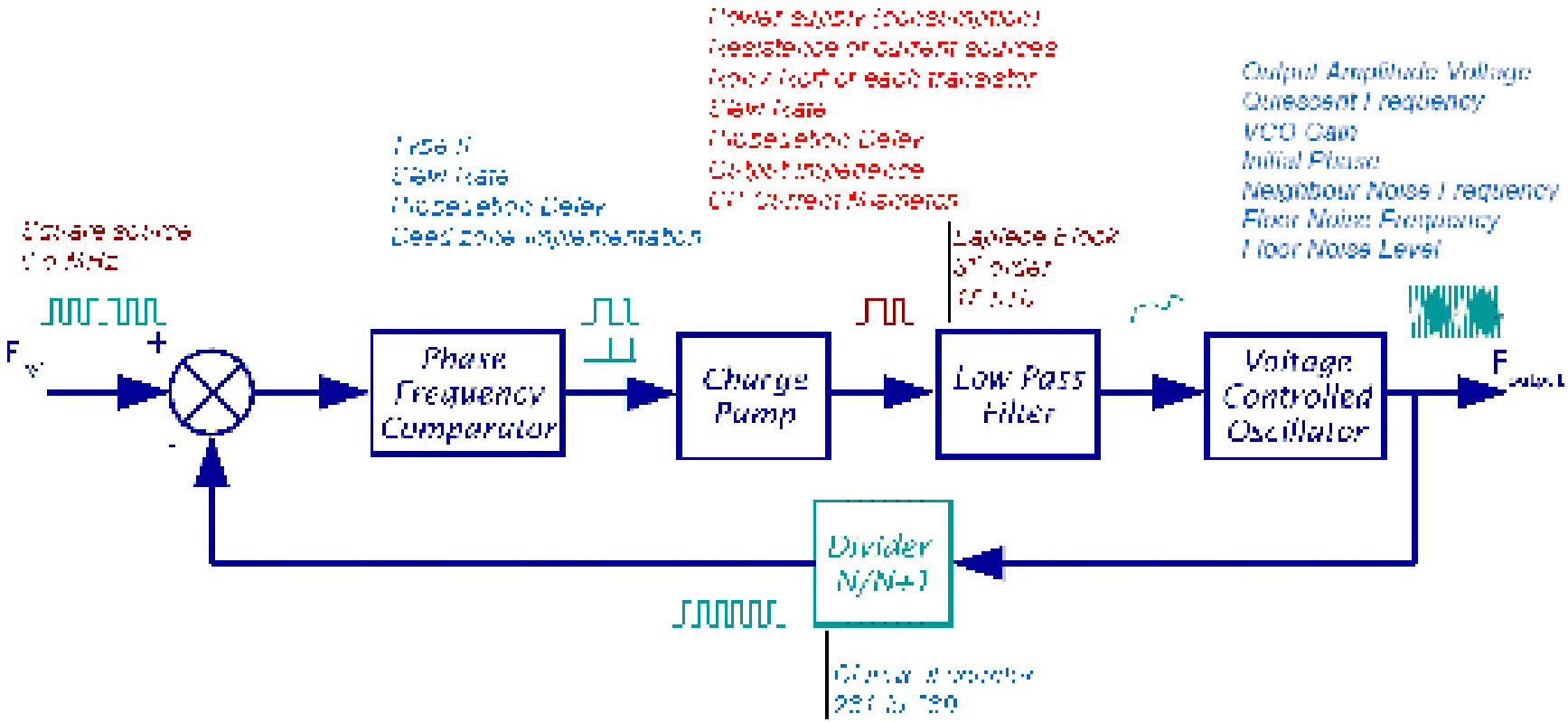
Application Presentation

- Application: DCS Standard
- N-Integer PLL

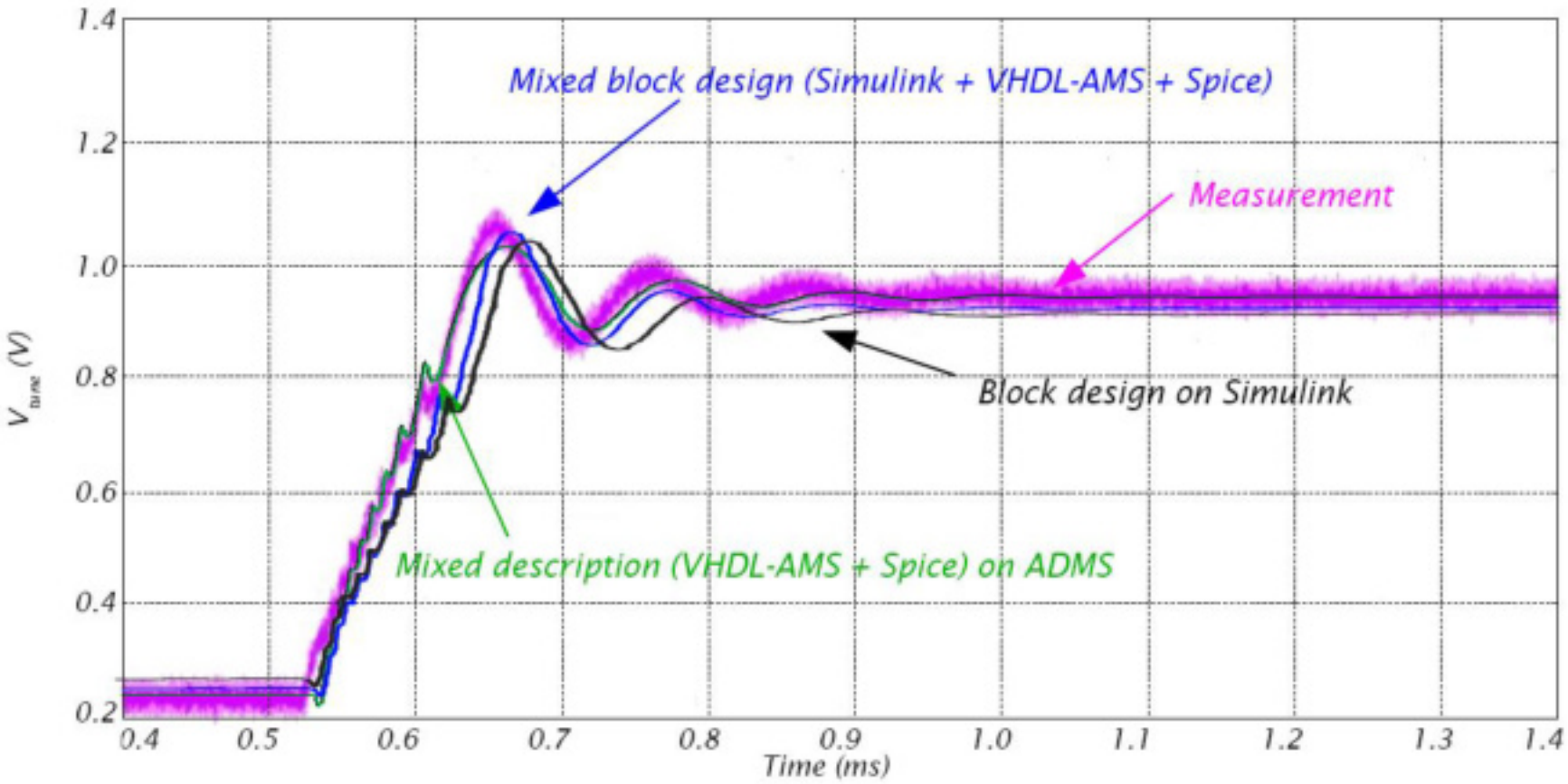


- Key numbers:
  - Fref = 6.5 MHz
  - N = 261/269
  - Ipump = 300 µA
  - LPF @ 15 kHz, 3rd order

Mixed Simulink PLL Simulation



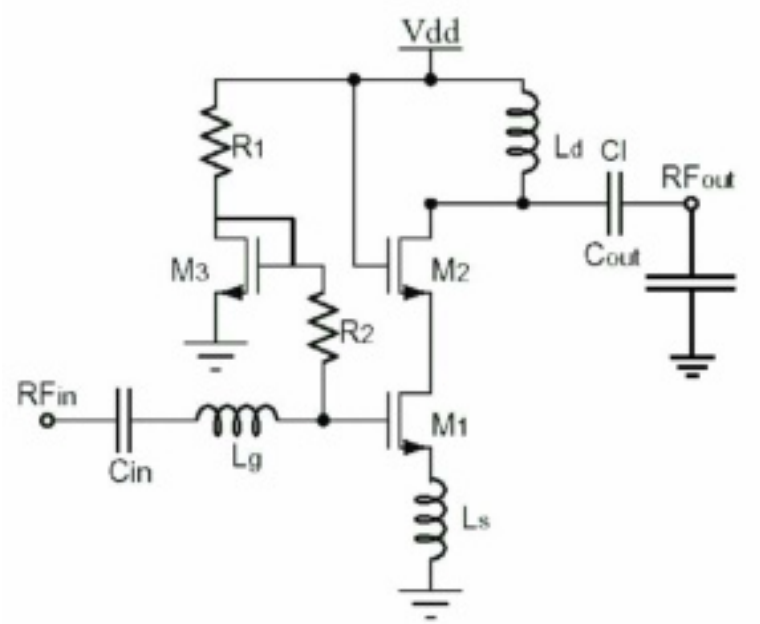
Mixed Simulink PLL Simulation



@ Simulink: ~ 4h
@ Exported on ADVance MS: ~ 2h
@ on ADVance MS: 40h
@ Mixed on ADVance MS: ~3h

LNA Modeling

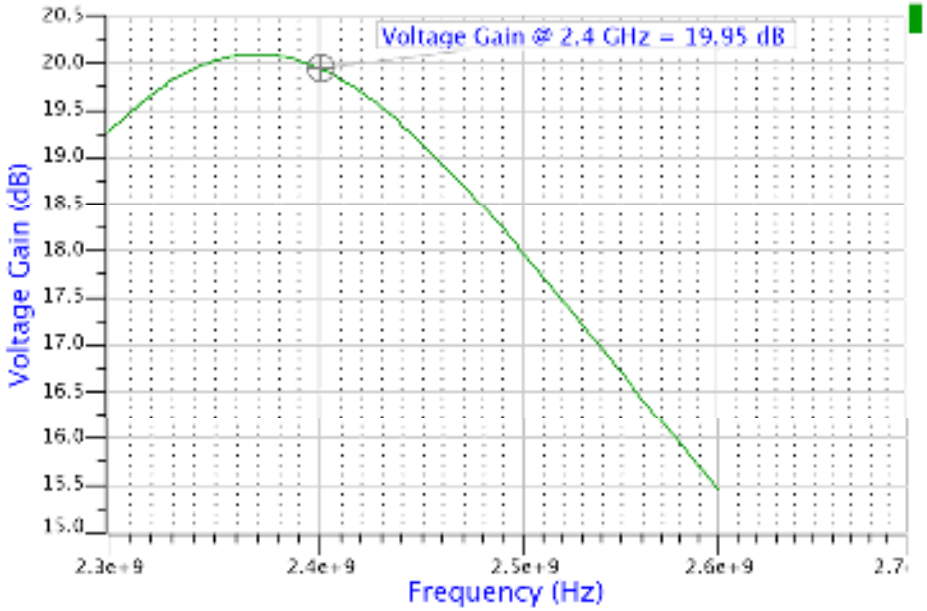
- Conception of a LNA in Spice @ 2.4 GHz
  - Simulink:
    - Power Gain
    - Input Impedance
    - Output Impedance
    - Compression Point
    - Noise Figure
    - Temperature
  - VHDL-AMS:
    - Power Gain
    - Input Impedance
    - Output Impedance
    - Compression Point
    - Bandwidth

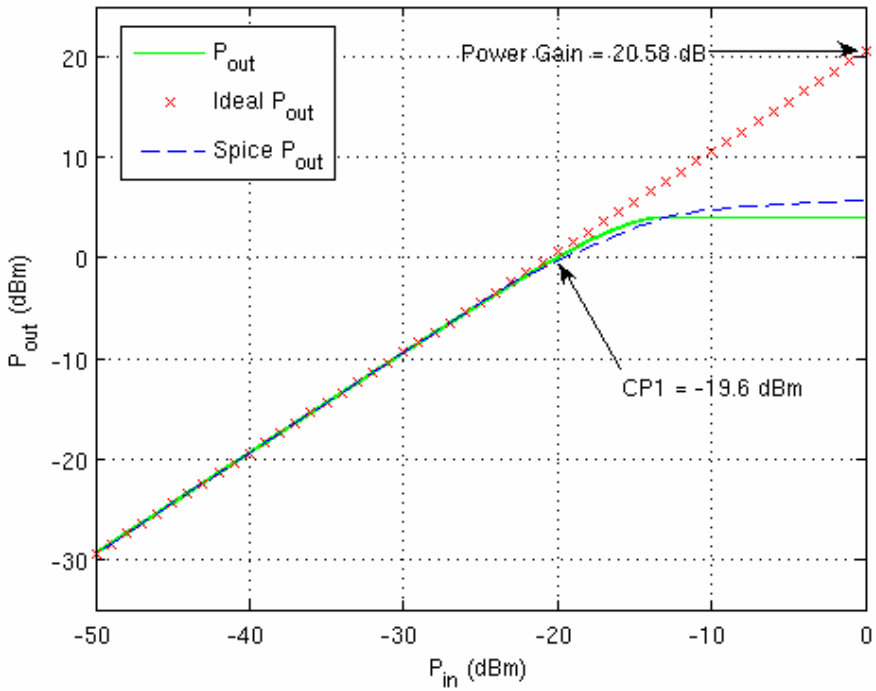


Parameters	*Simulation*
Power Gain	20.58 dB
ICP1	-19.6 dBm
Noise Figure	1.487 dB
Power	2.8 mW
Input Impedance	49.48 Ω
Output Impedance	50.09 Ω

LNA Modeling

- Results:





Simulation Time and Specifications

- Simulink Modeling

Channel	PA	RX Mixers	TX Mixers	LNA	TS (min)	Time (ms)	Bits	Processed	BER	TS/bit (s)	Hopping	Sampling	Obs.
Attenuation	Ideal Gain	Ideal Gain	Ideal Gain	Ideal Gain	30	1,816	1211	370	0,000	1,487	2	(0.1e-9)	
Attenuation	Gain + IP3	Ideal Gain	Ideal Gain	Ideal Gain	38	1,576	1051	210	0,000	2,170	2	(0.1e-9)	
Attenuation	Gain + IP3	Ideal Gain	Ideal Gain	Gain + IP3	49	1,550	1033	190	0,000	2,845	2	(0.1e-9)	
Attenuation	Gain + IP3	Ideal Gain	Gain + IP3	Gain + IP3	857	16,170	10780	9940	0,000	4,770	25	(0.1e-9)	
Attenuation	Gain + IP3	Gain + IP3	Gain + IP3	Gain + IP3	184	2,580	1720	870	0,000	6,419	4	(0.1e-9)	
Attenuation	Gain + IP3	Gain + IP3	Gain + IP3	Gain + IP3 + Noise	1420	2,045	1363	520	0,000	62,494	3	(0.01e-9)	NF=1.8dB
Attenuation	Gain + IP3	Gain + IP3	Gain + IP3	Gain + IP3 + Noise	5760	8,243	5495	4650	0,469	62,890	13	(0.01e-9)	NF=3dB

- Block Specifications

		TX Part						RX Part			
		I Mixer	Q Mixer	RF Mixer	BP RF	PA	LNA	IF Mixer	I Mixer	Q Mixer	LP IF
Gain (dB)	Archi.	5,00	5,00	5,00	Butterworth	21,00	26	10,000	10,000	10,000	Butterworth
IP3 (dBm)	Type	25,00	25,00	25,00	Bandpass	29,67	-5	10,000	10,000	10,000	Lowpass
NF	Order				3,00		1,8 / 290K				3,000
Zin	Freq 1	50,00	50,00	50,00	(2.4 100e6)	50,00	50	50,000	50,000	50,000	1,00E+07
Zout	Freq 2	50,00	50,00	50,00	(2.4 100e6)	50,00	50	50,000	50,000	50,000	1,00E+07

Conclusion

Conclusion

- Functional model of Bluetooth and WiMedia systems implemented in SystemC.
- Coupling Simulink/VHDL-AMS/Spice.
- Mixed hierarchical simulations.

- Future work : SystemC/VHDL-AMS simulation
  - Simulation of an application from the Software layers to the Radio layer.

Thank you for your attention