

# COSEDA Technologies User Group Meeting 2016

Modeling of an ADC for a RF Transceiver with COSIDE®

# Seamless Waves Semiconductors

#### Who we are

**ADC** 

2009

Seamless Waves provides effective solutions for agile reconfigurable RF Front End using new design techniques enabling ultra low power communication and an efficient bandwidth adaptation.

2011

2010

100MHz-1GHz and 1GHz-3GHz to serve military radio market, low power receiver for specific wearable market and spectrum sensing UPMC 3.0G applications.

**UPMC** 2.4G **UPMC** Tunable **UPMC** 2.4G ADC **Tunable** 0.9G Rx **ADC UPMC** 0.4G **ADC UPMC ADC** 2.4G 2015 2014 2013 **ADC** 2012

- 1

**UPMC** 

9.0G



# We have to exchange the executable specifications with customers

- As their systems are becoming bigger and complex we need to provide models early in the global architecture process
- Systemc AMS is a perfect candidate
  - Delivery can be compiled or provided with source code
  - Mix simulation and software driven application
- Simulator license issue for the end customers



# The choice of COSIDE® is meeting our requirements

- To accelerate our modeling flow (flat systemc ams or systemc files with multiples configurations)
  - But reuse our legacy from in Matlab Simulink
  - Software Driven Radio introduces many configuration issues
- ► To exchange with customers with meaningful representation
- ► To move to smart component and integrate digital
  - ▶ We need processor and software to drive the configuration of our ADCs and Radio Receiver
  - Simulink was not an option here
- ▶ To enable virtual tests/instruments usage for system companies early in the design process

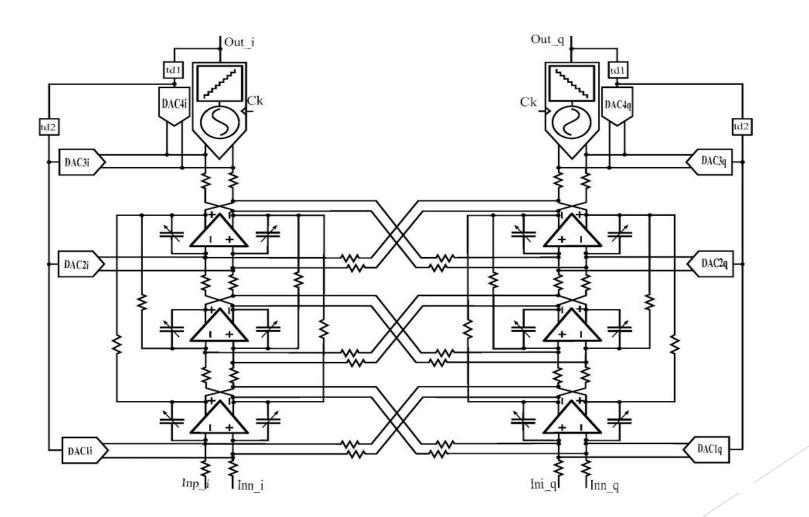


# Seamless Waves Background in Modeling

- ► For our new project the team is composed with 1 SystemC AMS expert involved since 2008 with ESL standards and 4 analog/RF designers
  - Expertise is coming from
    - Wasabi European project
    - ▶ BDREAMS European project
  - Last 3 ASICs were used with Systemc Ams modeling
    - Experiment : Validation
    - Experiment : Characterization (back annotation)
    - ▶ Post-Silicon Chip validation ( to be done with the new coseda bridges to Keysight)

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# Use Case: Modeling a Quadrature Sigma-Delta Modulator

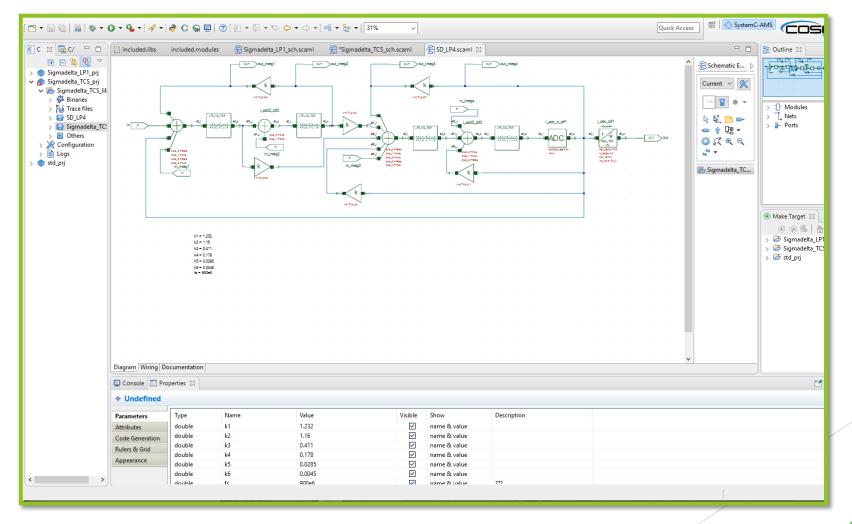


# igma-

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## Use Case: Modeling a Quadrature Sigma-Delta Modulator



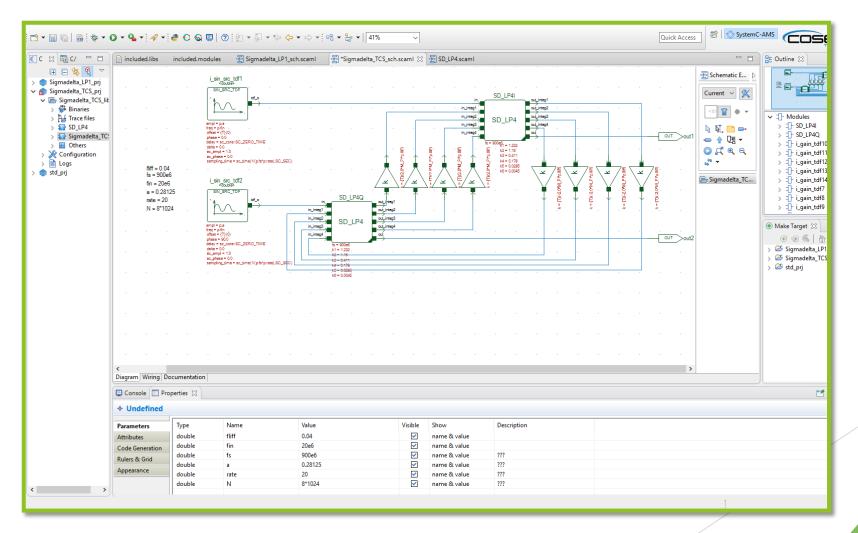


#### Benefits

- We were able to use directly RF basic modules from of a large library.
  - ▶ No need to reinvent the wheel or to redefine Systemc AMS basic blocks
  - ► Library understandable by analog/rf designers
  - ► Clear understanding between architect and designers
    - ► Same schematic, same concepts
    - ► SystemC code is accessible and editable

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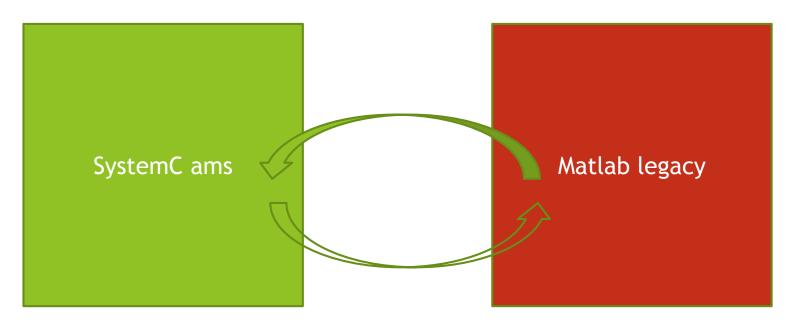
Use Case: Modeling a Quadrature Sigma-Delta Modulator - introducing environment and stimuli





### Testbench with Matlab legacy

- Reuse of legacy analysis in matlab (dump of plots using .dat file)
- Import of waveforms coming from RF specific modules made with matlab at a certain time.
- SystemC AMS used as scheduler for our testbench





# (Eclipse) Plugin inside COSIDE®

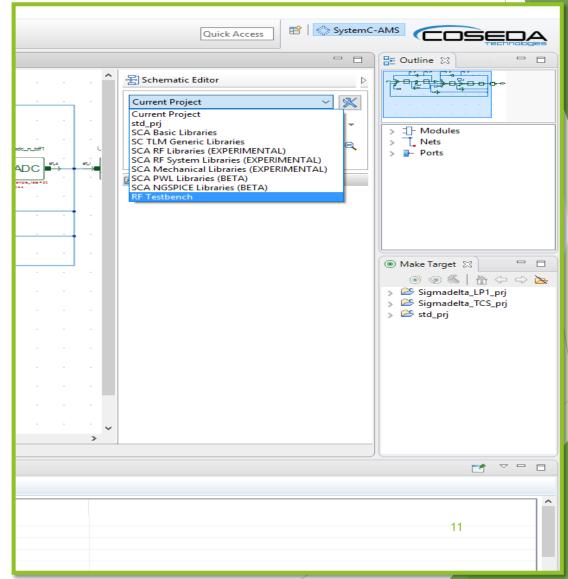
Eclipse plugin (extendable, expandable)
Portable java on both windows or linux

#### Classical RF Inputs:

- -2 tone test
- -Noisy channel (channel modeling)

#### **Output Analysis**

- -RF eye diagram
- -Bit error rate
- -Specific Constellation (octave)
- -Spectrum analysis (octave)





### Mix digital and analog

Sensors modeled in SystemC ams

RF modeled in SystemC ams

Filters SystemC Do we need accuracy? in our case no
We need to ship the executable specifications

CPU and Micro
Controller
ARM Fast models,
IMPERAS/OVP,
QEMU GreenSocs...



### Next steps

- ► COSIDE® to virtuoso bridges will be used
  - ▶ We will change our flow to introduce this feature
  - ► Elaboration of the configuration? Who is driving the coherency?
- Greensocs QEMU integration
  - ► To drive the configuration
  - Reuse of firmware (continuous integration)

# THANK YOU

