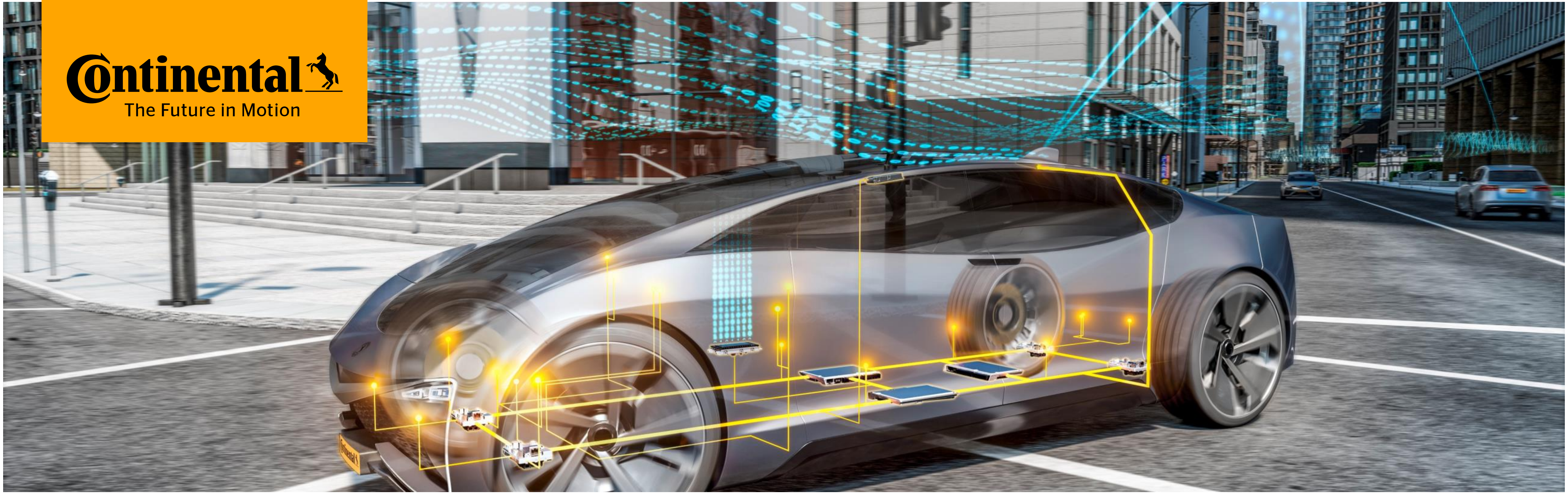


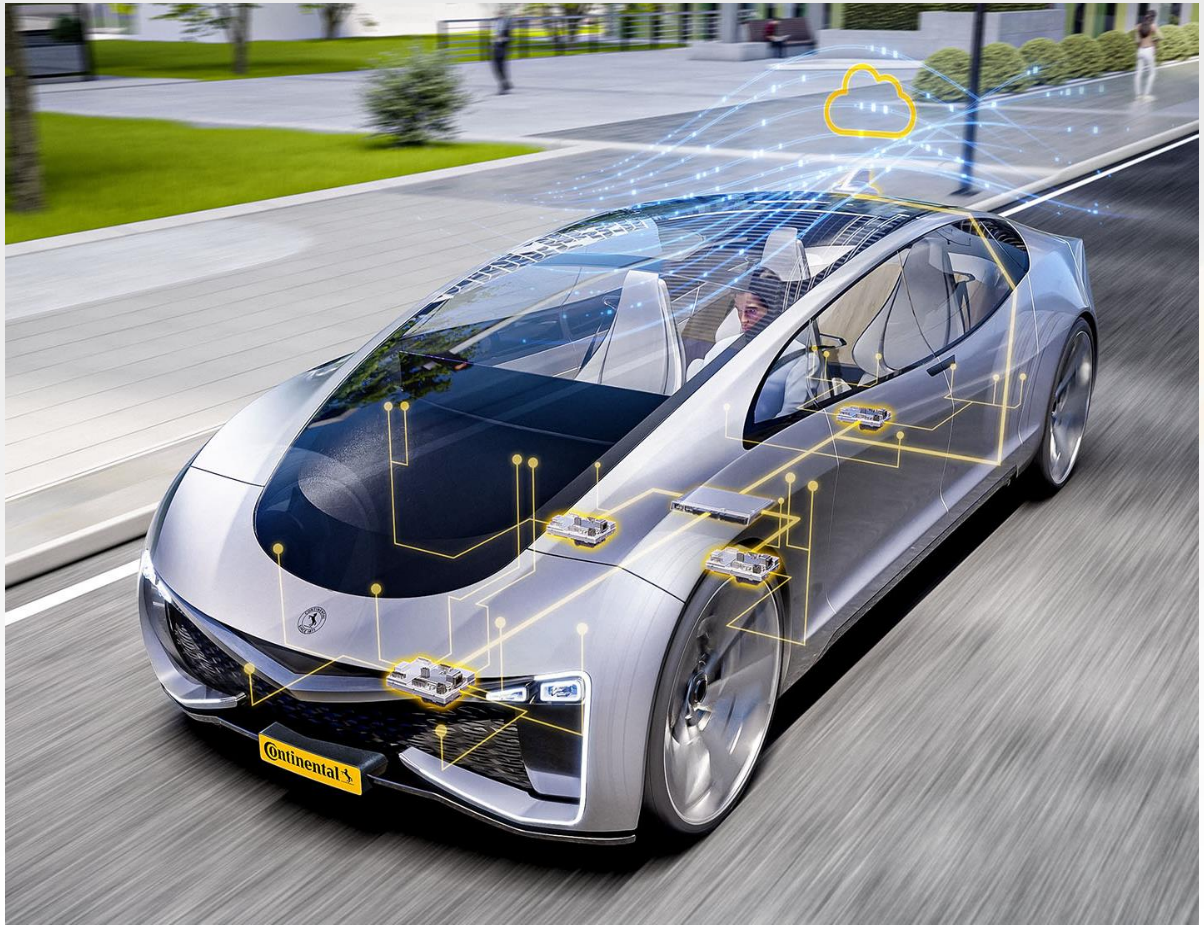
Reusing Generic C-Peripheral Models in L4 SystemC Simulation

Agenda

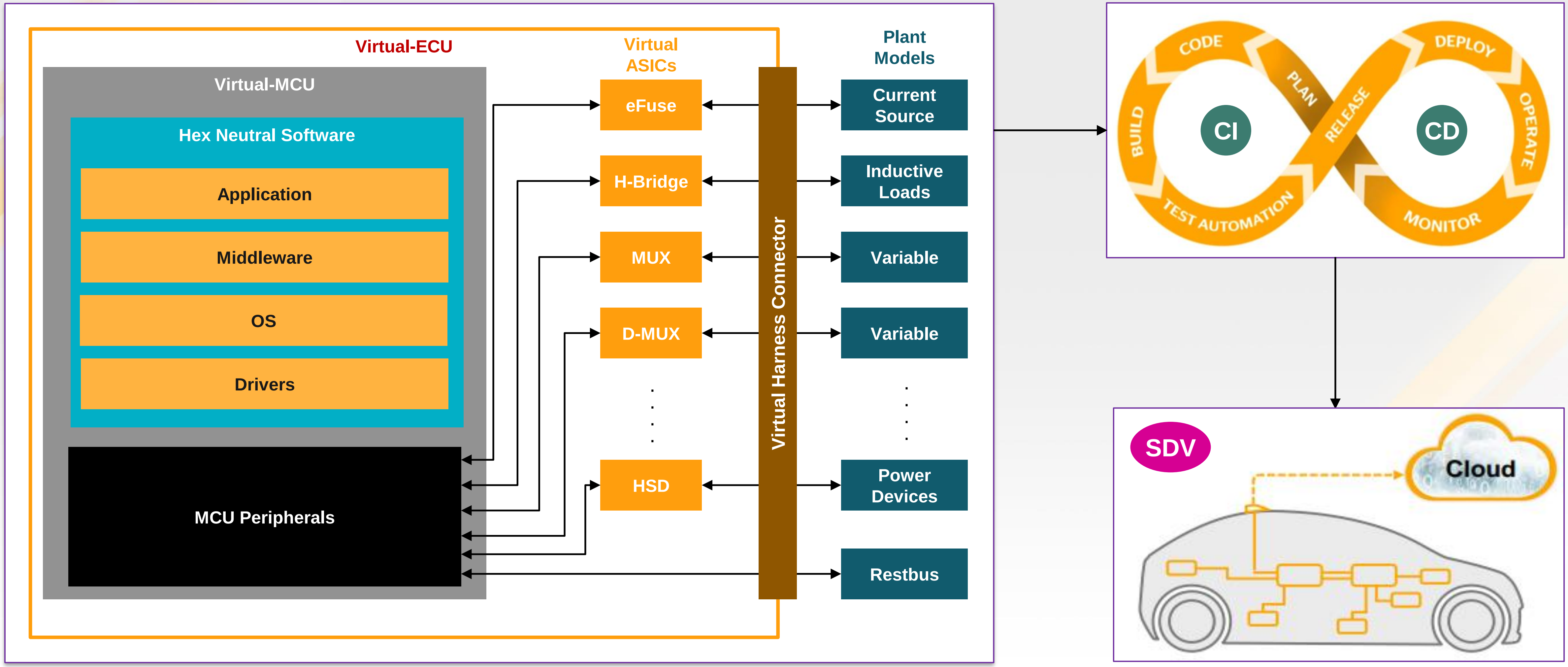
Agenda

Purpose

- Virtual-ECU development to run the unmodified binary (L4 Simulation).
- Assist Software Defined Vehicle Development with Virtualization.
- Reuse Peripheral’s C-model from higher abstraction level (L3 vECU) in L4 Simulation.
- Create a generic L4 framework, which could be re-used in other vendors framework.
- Provide a scalable solution for L4 vECU development.



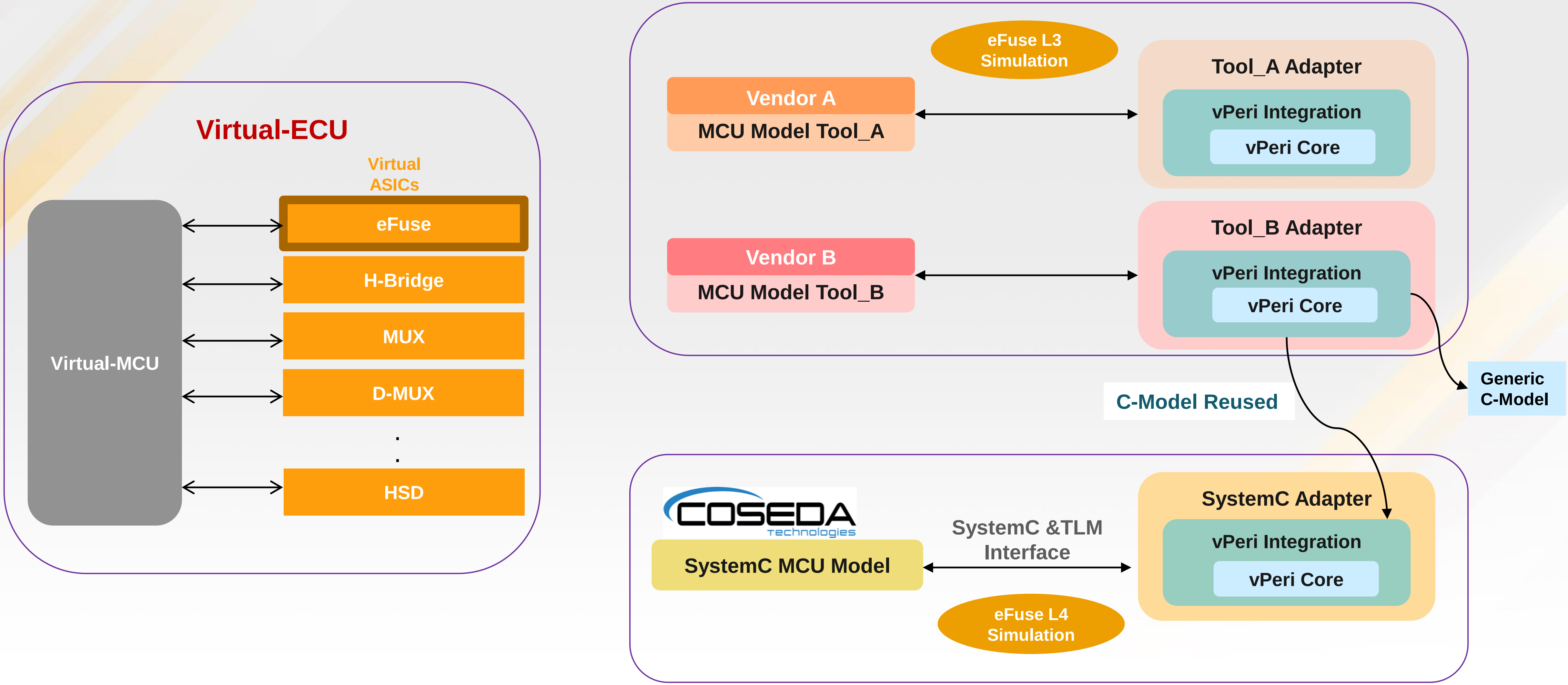
Big Picture



Virtual-ECU
Virtual ASICs
Plant Models
Virtual-MCU
Hex Neutral Software
Application
Middleware
OS
Drivers
MCU Peripherals
eFuse
H-Bridge
MUX
D-MUX
HSD
Virtual Harness Connector
Current Source
Inductive Loads
Variable
Variable
Power Devices
Restbus
CODE
PLAN
RELEASE
DEPLOY
OPERATE
MONITOR
TEST AUTOMATION
BUILD
CI
CD
SDV
Cloud

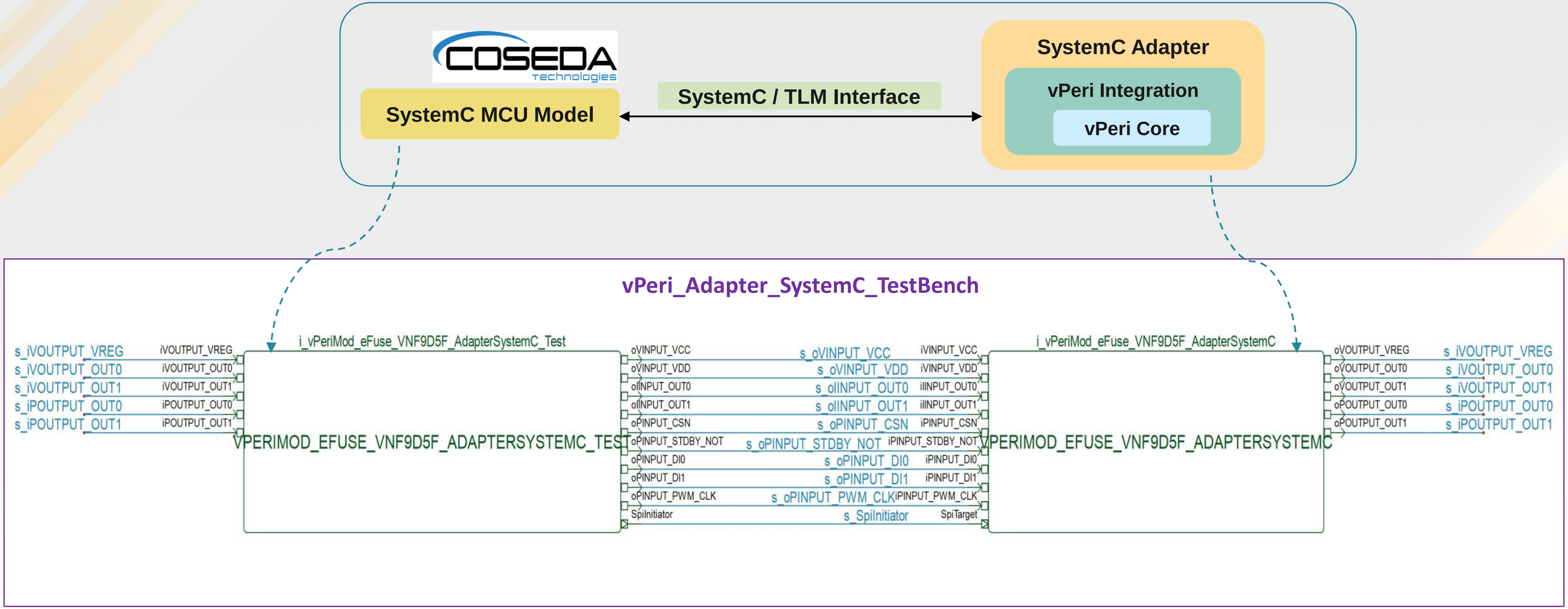
Agenda

Reusing C-models



Agenda

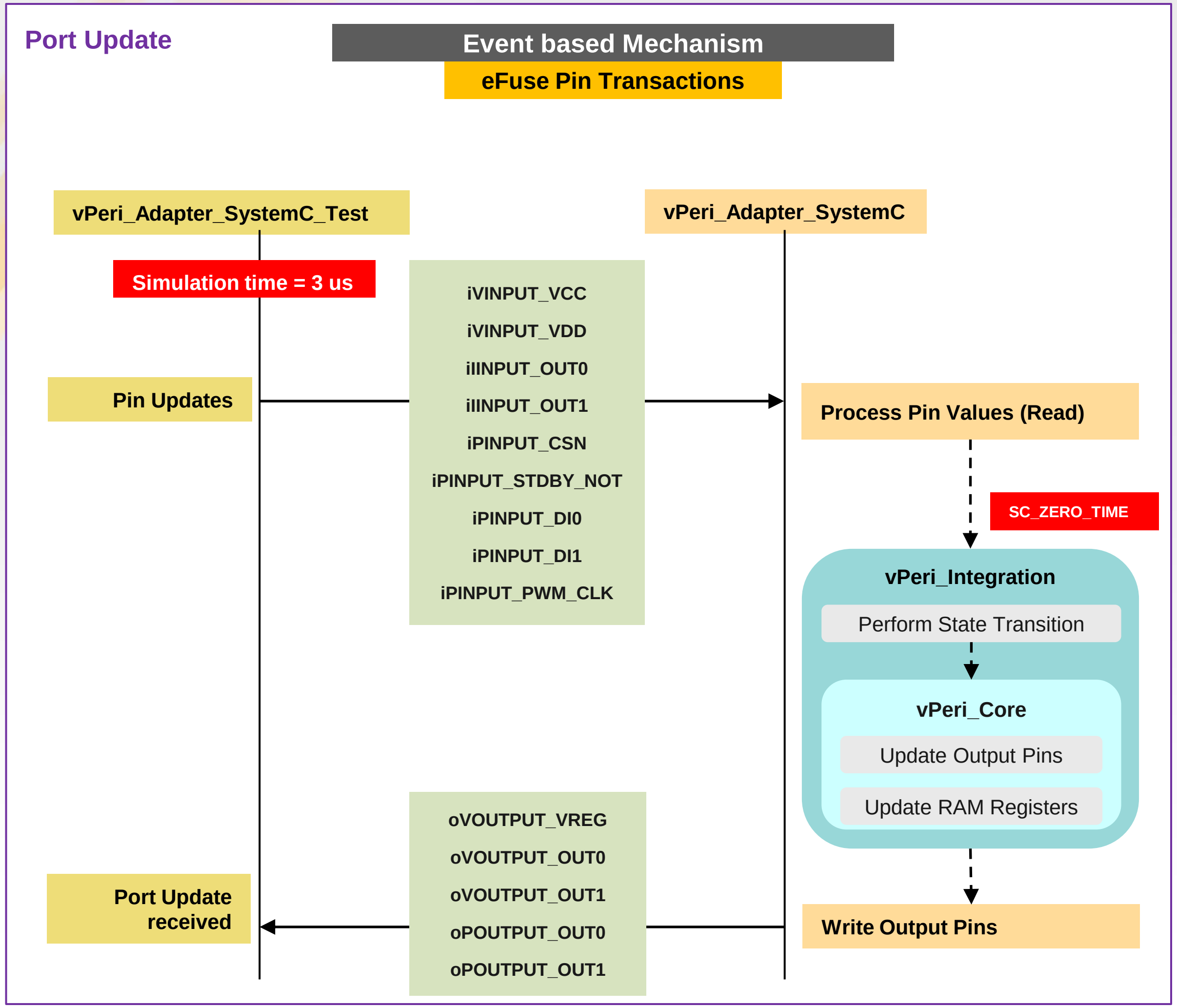
Schematic & Testbench Setup

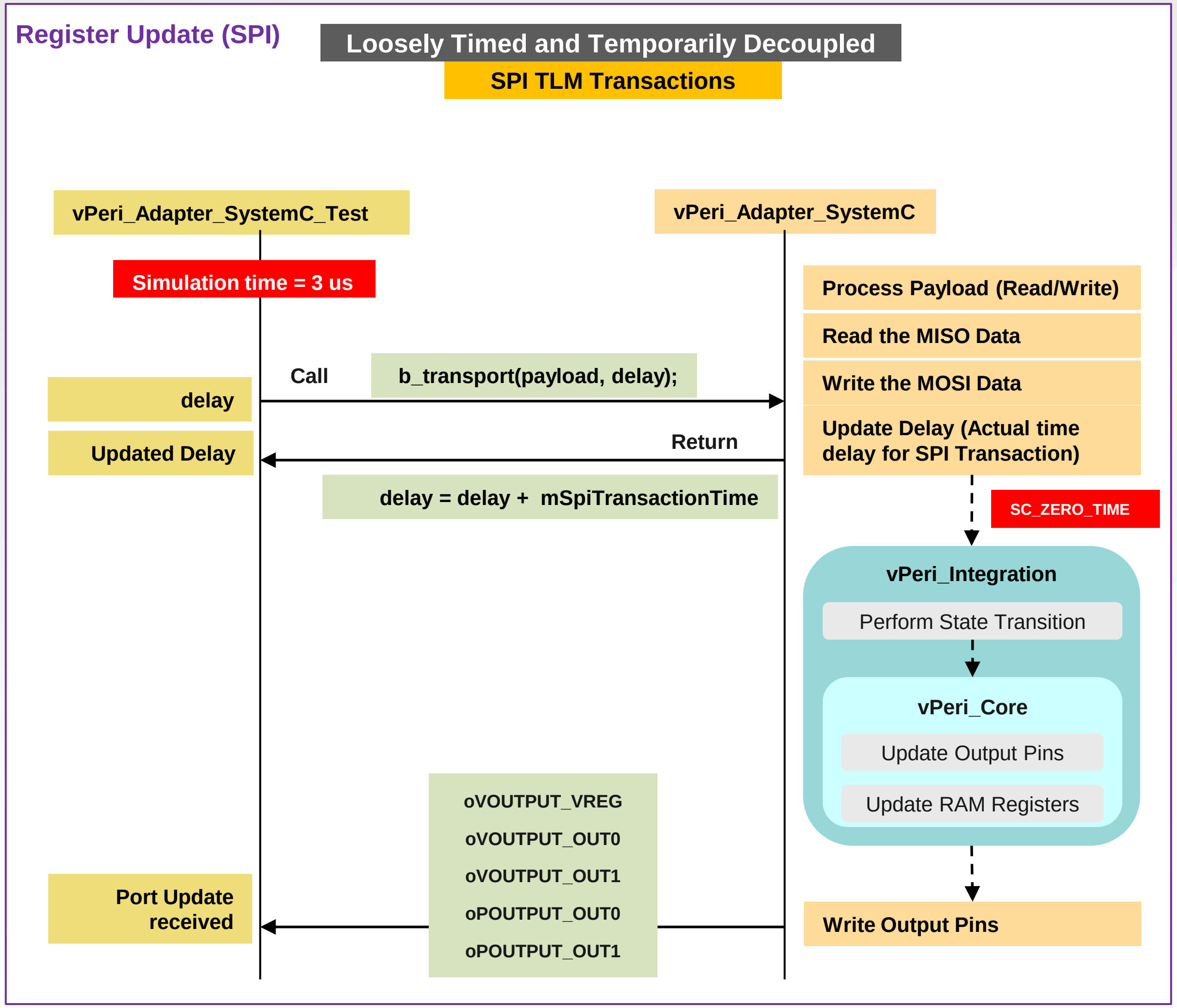


Agenda

SystemC Adapter Design

- SystemC and TLM implementation
- Not vendor specific





Agenda

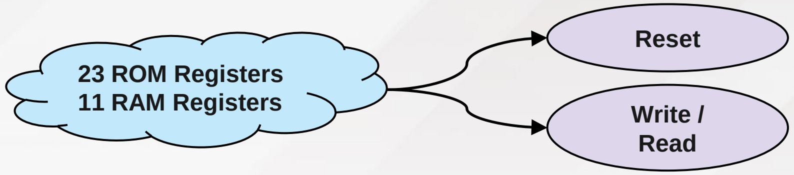
SystemC Adapter Verification

Integrated external test library into COSIDE

Port Reset Test

```
------------- Start Test Case : PortResetTest @ 1 us -------------
Pass : Port Name = iVOUTPUT_OUT0, Read Reset Value = 0.000000
Pass : Port Name = iVOUTPUT_OUT1, Read Reset Value = 0.000000
Pass : Port Name = iVOUTPUT_VREG, Read Reset Value = 4.500000
Pass : Port Name = iPOUTPUT_OUT0, Read Reset Value = 0
Pass : Port Name = iPOUTPUT_OUT1, Read Reset Value = 0
------------- End Test Case: PortResetTest @ 1 us -------------
************* Test Case Summary : PortResetTest *************
Test Result          =  PASS
Total No. of tests  =  5
No. of tests Passed =  5
No. of tests Failed =  0
***********************************************************
```

Register Reset Test




```
------------- End Test Case: RegisterResetTest @ 2340 ns -------------
************* Test Case Summary : RegisterResetTest *************
Test Result          =  PASS
Total No. of tests  =  34
No. of tests Passed =  34
No. of tests Failed =  0
*******************************************************
```

```
------------- End Test Case: RegisterWriteReadTest @ 4020 ns -------------
************* Test Case Summary : RegisterWriteReadTest *************
Test Result          =  PASS
Total No. of tests  =  34
No. of tests Passed =  34
No. of tests Failed =  0
*****************************************************
```

State Transition Test

Failsafe_to_PrestandbyMode_Test Output

```
------------ Start Test Case : Failsafe_to_PrestandbyMode_Test @ 5020 ns ------------
Pass : Port Name = iVOUTPUT_OUT0, Read Expected Value = 0.000000
Pass : Port Name = iVOUTPUT_OUT1, Read Expected Value = 0.000000
Pass : Port Name = iVOUTPUT_VREG, Read Expected Value = 4.500000
Pass : Port Name = iPOUTPUT_OUT0, Read Expected Value = 0
Pass : Port Name = iPOUTPUT_OUT1, Read Expected Value = 0
------------ End Test Case: Failsafe_to_PrestandbyMode_Test @ 5020 ns ------------
************ Test Case Summary : Failsafe_to_PrestandbyMode_Test ************
Test Result          =  PASS
Total No. of tests  =  5
No. of tests Passed =  5
No. of tests Failed =  0
*****************************************************
```

Standby_to_FailsafeMode_Test Output

```
------------ Start Test Case : Failsafe_to_NormalMode_Test @ 7020 ns ------------
Pass : Reg Addr = 0x14, Read Value = 0x800, Read Global Status Byte = 0x80
Pass : Reg Addr = 0x14, Read Value = 0x800, Read Global Status Byte = 0x80
Pass : Port Name = iVOUTPUT_OUT0, Read Expected Value = 0.000000
Pass : Port Name = iVOUTPUT_OUT1, Read Expected Value = 0.000000
Pass : Port Name = iVOUTPUT_VREG, Read Expected Value = 4.500000
Pass : Port Name = iPOUTPUT_OUT0, Read Expected Value = 0
Pass : Port Name = iPOUTPUT_OUT1, Read Expected Value = 0
------------ End Test Case: Failsafe_to_NormalMode_Test @ 8060 ns ------------
************ Test Case Summary : Failsafe_to_NormalMode_Test ************
Test Result          =  PASS
Total No. of tests  =  7
No. of tests Passed =  7
No. of tests Failed =  0
*****************************************************
```

Failsafe_to_NormalMode_Test Output

```
------------ Start Test Case : Failsafe_to_PrestandbyMode_Test @ 5020 ns ------------
Pass : Port Name = iVOUTPUT_OUT0, Read Expected Value = 0.000000
Pass : Port Name = iVOUTPUT_OUT1, Read Expected Value = 0.000000
Pass : Port Name = iVOUTPUT_VREG, Read Expected Value = 4.500000
Pass : Port Name = iPOUTPUT_OUT0, Read Expected Value = 0
Pass : Port Name = iPOUTPUT_OUT1, Read Expected Value = 0
------------ End Test Case: Failsafe_to_PrestandbyMode_Test @ 5020 ns ------------
************ Test Case Summary : Failsafe_to_PrestandbyMode_Test ************
Test Result          =  PASS
Total No. of tests  =  5
No. of tests Passed =  5
No. of tests Failed =  0
*****************************************************
```

Agenda

Advantages of using Coside

Open Standard

Offers SystemC & TLM based simulation without any vendor specific flavor

Reusability

The Generated code could be **reused** in different platforms without much modifications

Simplifies Library Integrations

Supports **integration** of external libraries & enhances reusability in layered architectures

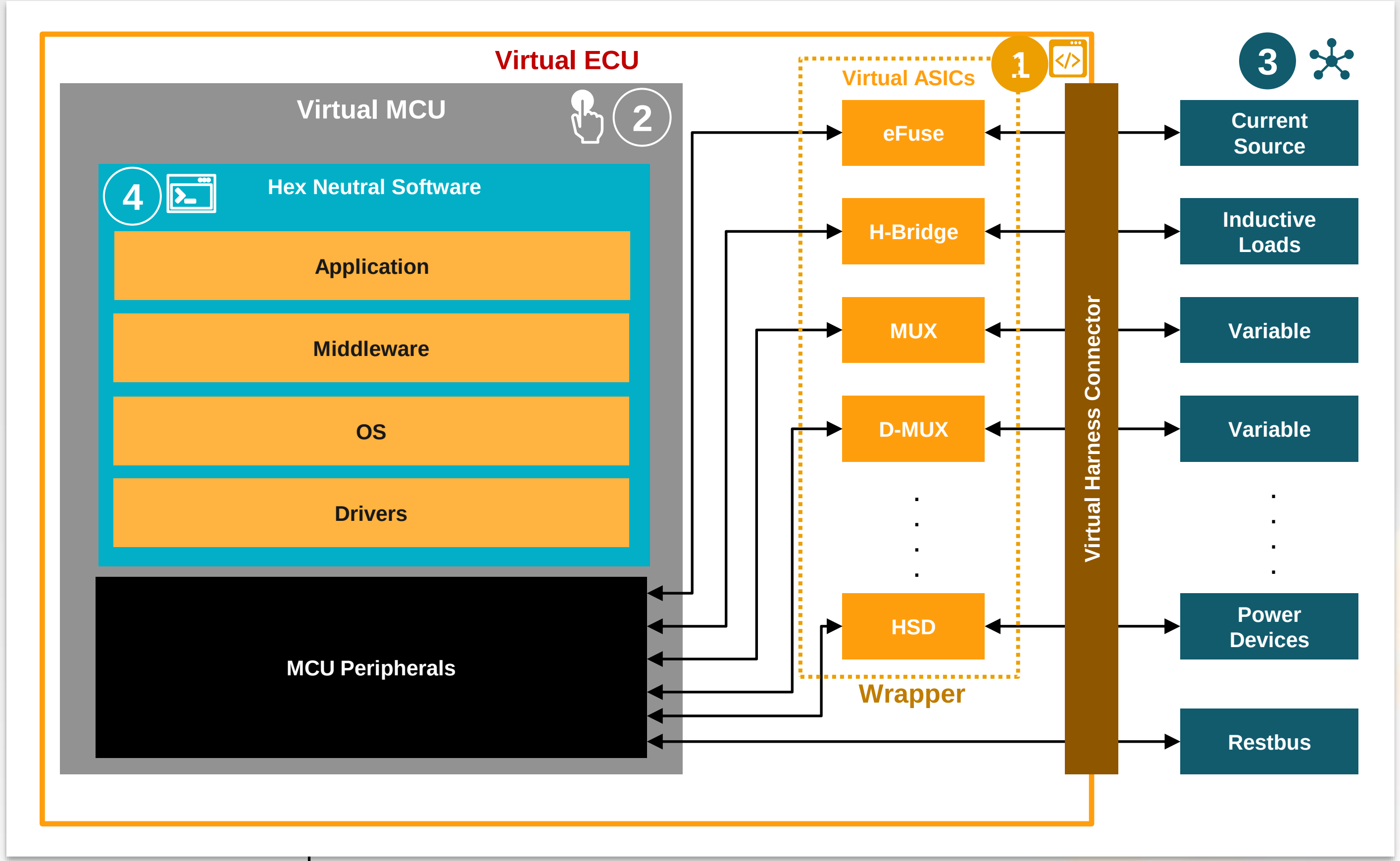
Minimal Development Time

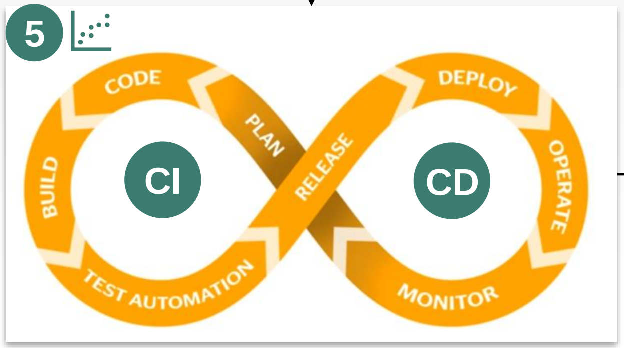
Code generation **simplifies & reduces** the efforts to create models.

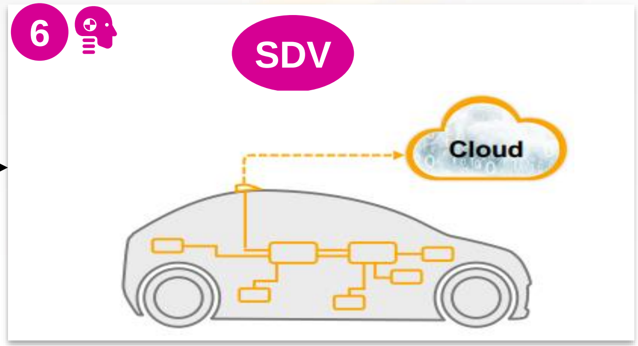
Agenda

Future Scope

1. Implement Wrapper around 'SystemC Adapter' for vendor specific simulation environment.
2. Use the virtual peripheral implementation in simulation environment to form L4 Virtual-ECU.
3. Connect the Plant Models to the Virtual-ECU via virtual harness connector.
4. Execute & validate the Hex Neutral Software in the L4 Virtual-ECU environment.
5. Integrate it in CI/CD Environment – To aid regression Testing.
6. Use this Platform to accelerate SDV development.







Thank You!!