swissbit

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Coseda User Group

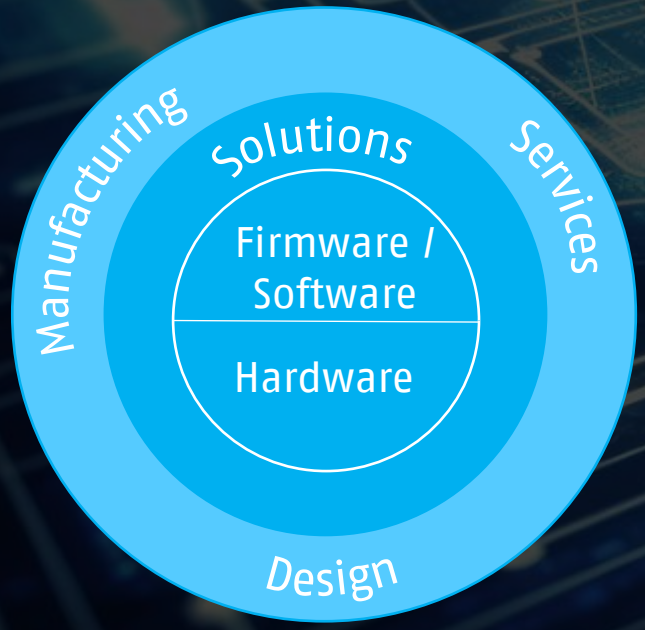
Steve Prigg

Store. Secure. Trust.

Swissbit Company Overview

- **Founded 2001**
- **~450 Employees**
- **Data Storage and Security Solutions**
  - NAND Flash Products (SSDs, Cards, USB, ...)
  - Security Products
- **Key Segments:**
  - Industrial, Enterprise&Networking, Edge Computing, Transportation, Medical, Financial
- **Sites:**
  - Switzerland (Bronschhofen HQ)
  - Germany (Berlin, Konstanz, Düsseldorf, Munich)
  - USA, Japan, Taiwan
- **Advanced Packaging, Manufacturing and Test Facility in Berlin**
  - ~200 employees
- **WWW:** www.swissbit.com

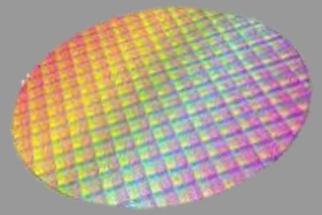
Providing full control of value chain



Assets

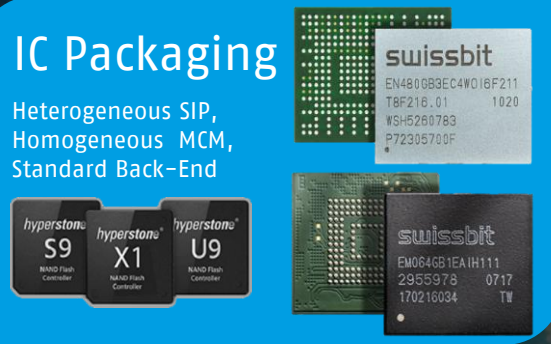
Skills

Wafer



IC Packaging

Heterogeneous SIP,
Homogeneous MCM,
Standard Back-End



Controller / FW / Packaging / Device design by Swissbit

System Assembly & Test

Customers

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“System in Package” in Berlin, Germany

3.200m²
PCB & Substrate material / year

>1.300
finished Product Variants

>150
active Hardware Variants

70%
of produced products are SiP designs

320km
of Bondwire / year

256M
SMD components (caps / res) / year

10.000
12 inch Wafer processed / year

High-quality Manufacturing and Mass Customization

Established

2002 Swissbit Germany AG

2019 New fab on 10.000m² incl. clean room

Made in Germany

Production

2 million units per month depending on product mix

Advanced 3D semiconductor Packaging, Test, BI, Data- & Certificate upload

Shift system

24/7 - 5 shift system

Certifications

ISO 9001:2015 – IATF 16949 – ISO 14001 – ISO 27001 – ISO 50001

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The Semiconductor Industry Is at an Inflection Point!

Higher complexity enabled by ➔ divide and conquer"

System Complexity

Predicted by Gordon Moore

"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected."

SysMoore Era (System)

System-In-Package

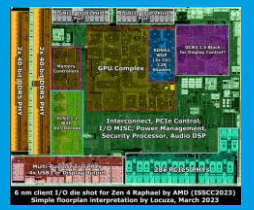
- Consumer
- Networking
- HPC/Data Center
- Mobile
- IoT / Edge
- Automotive
- Memory

Complexity gap

- Compute Performance
- Data Throughput
- Memory

Moore's Law (Silicon)

Moore's Law is slowing down…



System-On-Chip

Time

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Why Chiplets are Reshaping the Future of Custom Silicon

Benefits

Scalable Interoperability

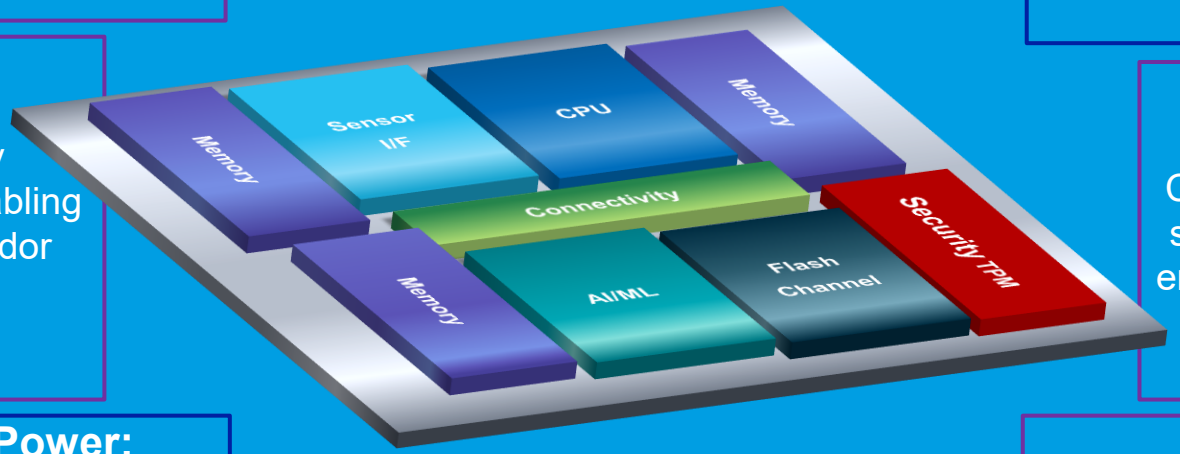
Chiplets enable a modular, standards-based approach that supports flexible integration, future-proofing, and cross-industry compatibility.

Cost-Performance Optimization

They allow targeted innovation across subsystems, helping balance performance and cost more efficiently than monolithic designs.

Ecosystem Collaboration

Chiplets drive industry alignment by encouraging reuse of proven IP and enabling critical standards that foster cross-vendor integration.



Enhanced Security

Chiplet architectures support tailored security measures to protect against emerging threats in complex systems.

Optimized Performance and Power:

Chiplets can be optimized for their specific functions and technologies, improving the SoC's performance and power efficiency. Chiplets can also be placed closer together, reducing the interconnects' latency and power consumption.

Design Flexibility

They unlock greater architectural freedom, allowing developers to customize systems for specific workloads and market needs.

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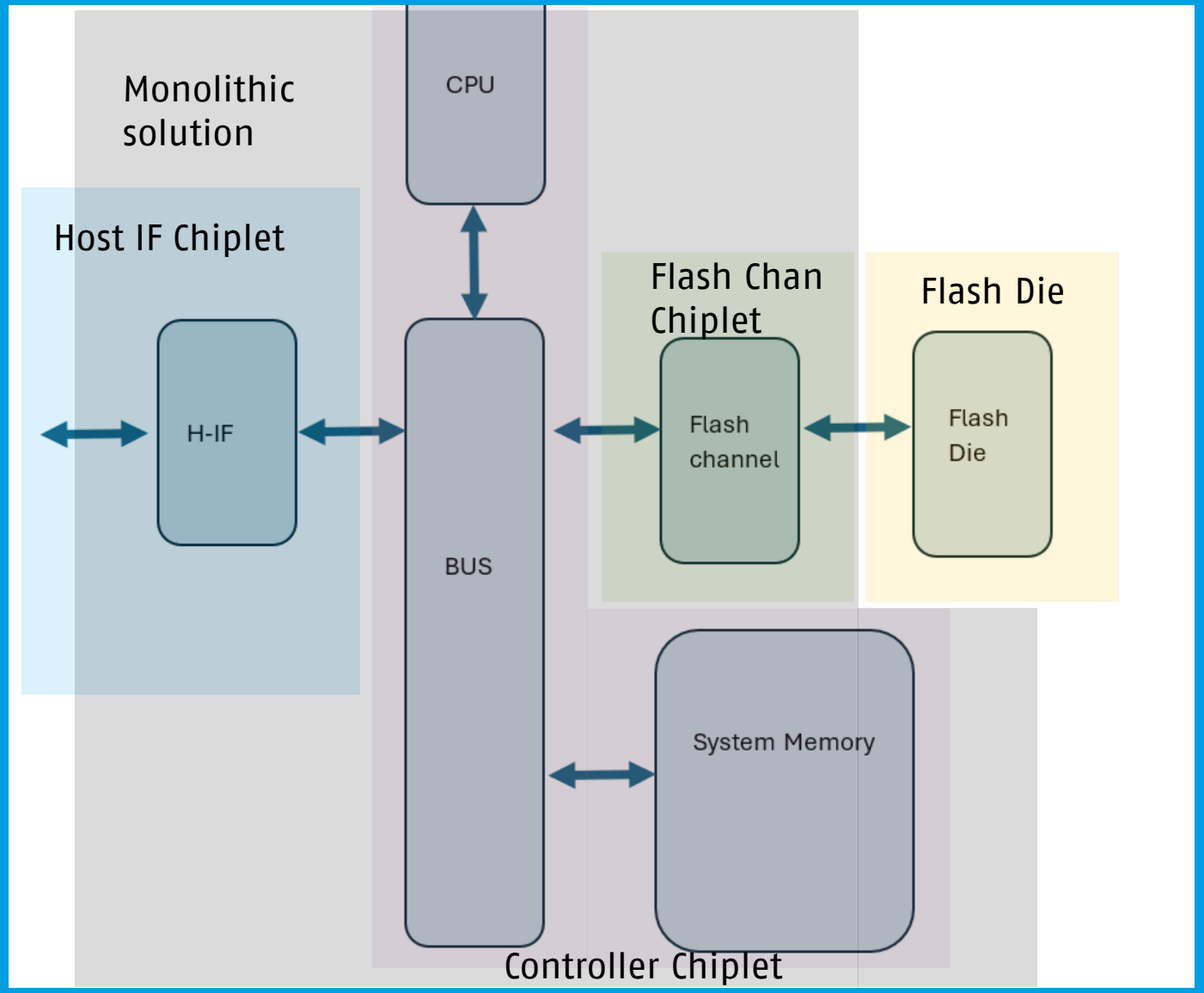
Flash Controller Concept

Topology

Host IF – developing fast

Flash Storage – developing fast



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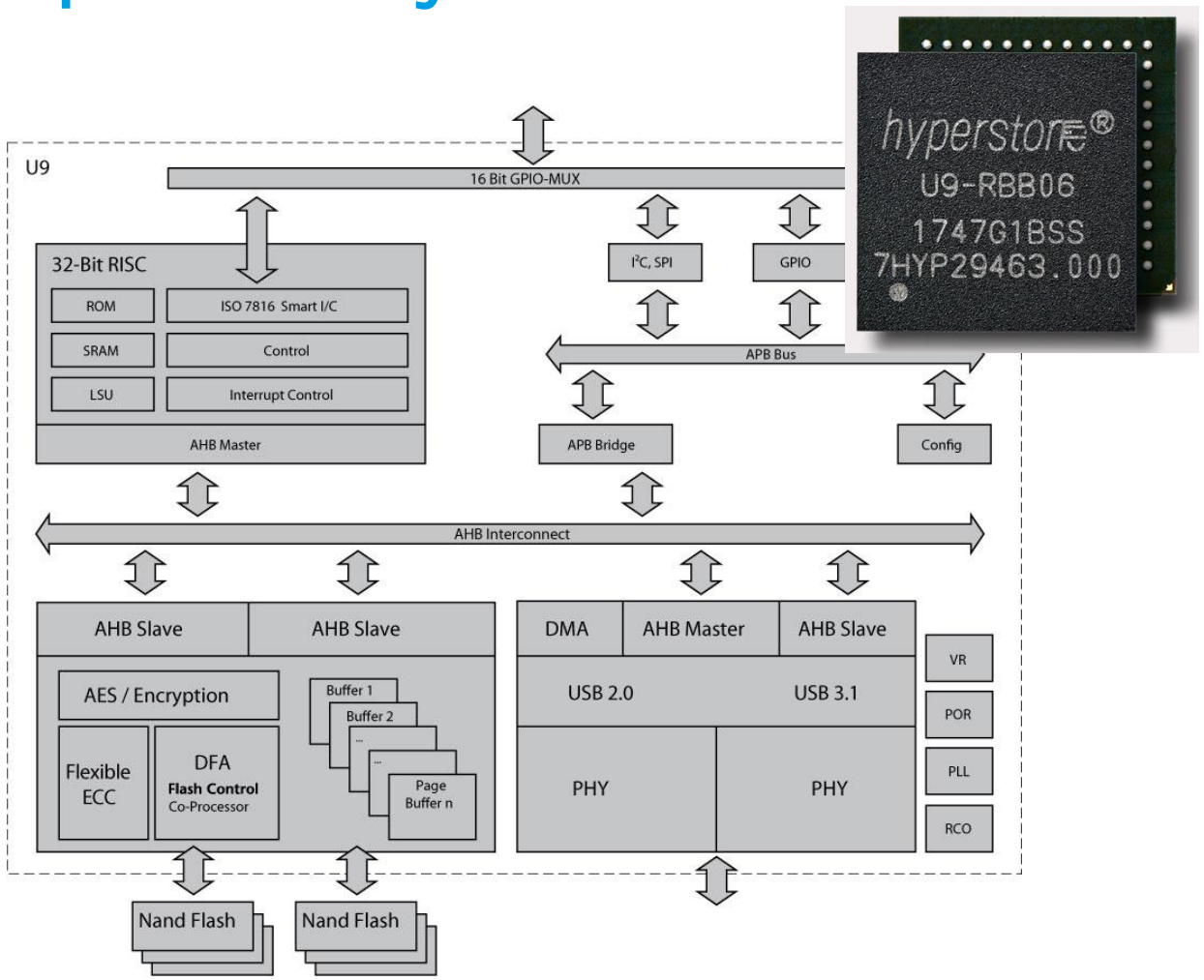
Shift from Monolithic to Chiplet Ecosystem

- **Traditional: Monolithic**
  - E.g.: Hyperstone USB 3.1 NAND Flash Memory Controller
- **Next-Gen Products:**
  - Shift to Chiplet-based Platforms
- **→IO Hub Controller as Central Processing Entity**



Hyperstone U9 USB 3.1 NAND Flash Controller

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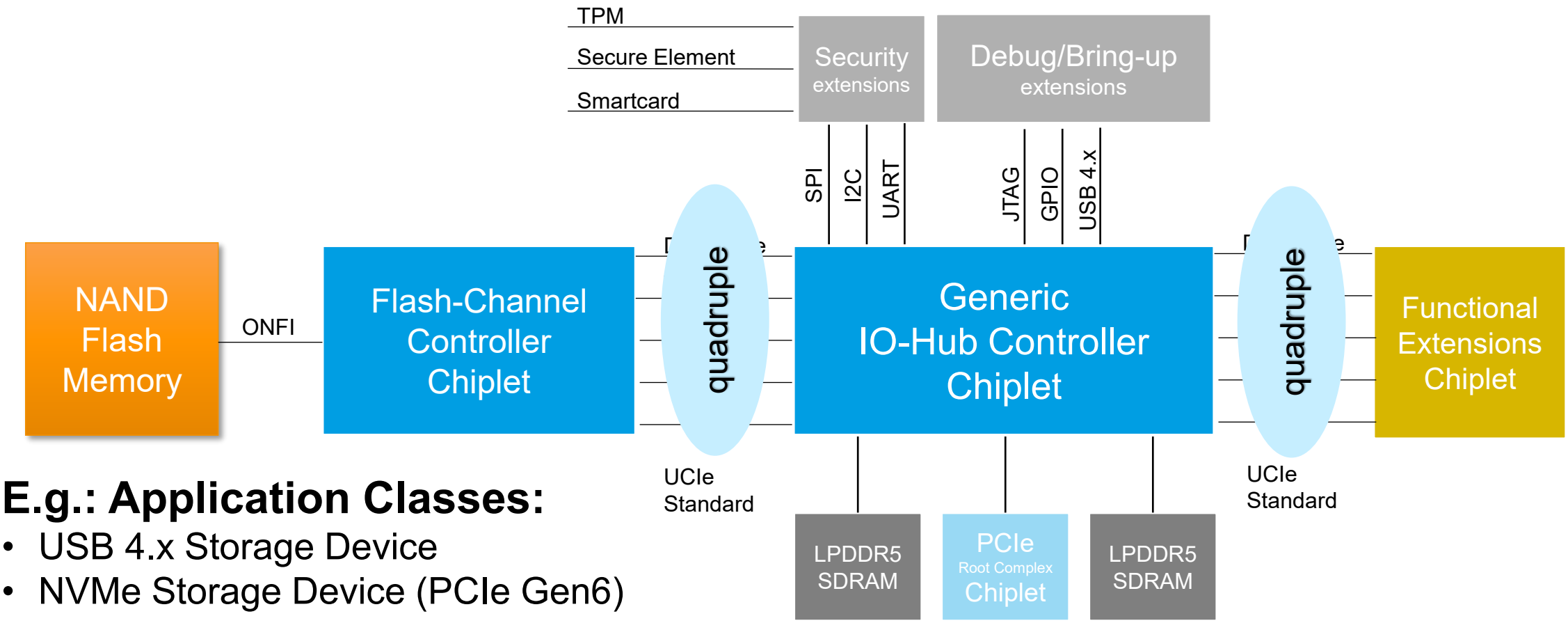
Universal Base Controller Chiplet – Chiplet ECOsystem



E.g.: Application Classes:

- USB 4.x Storage Device
- NVMe Storage Device (PCIe Gen6)

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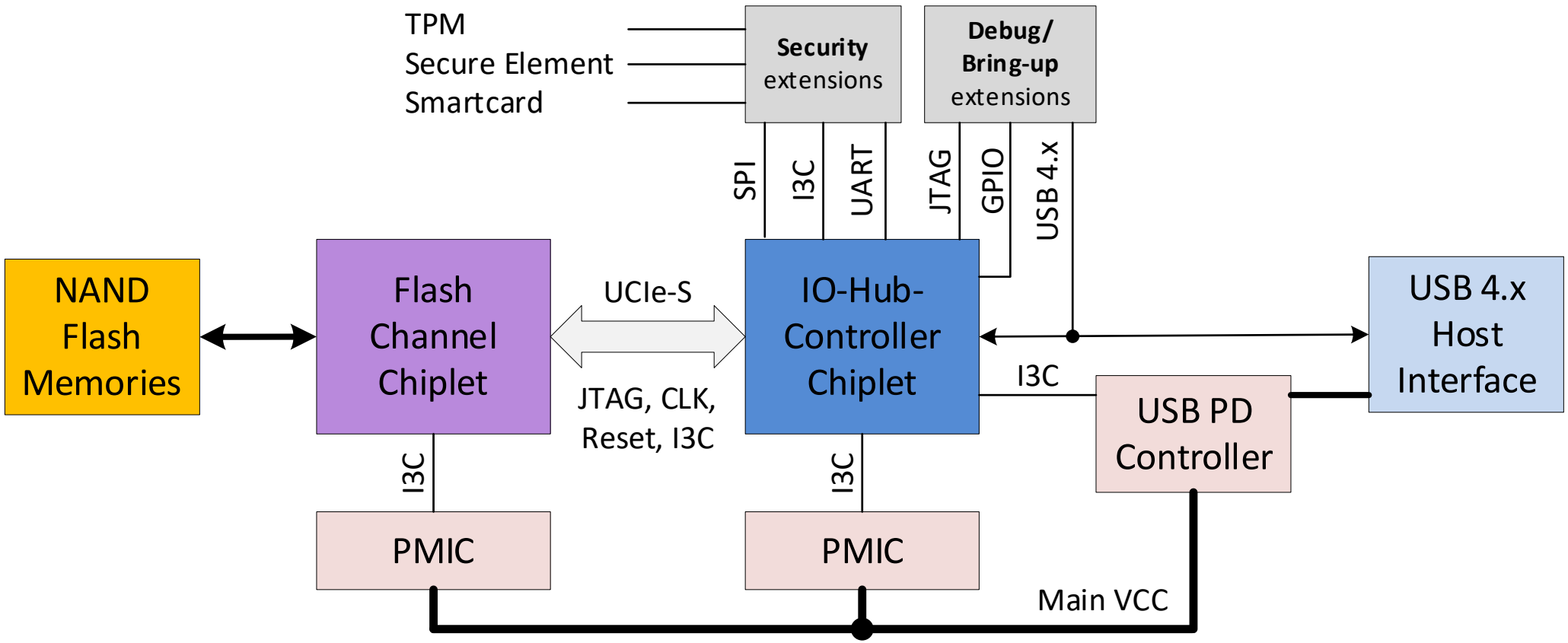
Use Case Example – USB4 Storage Platform



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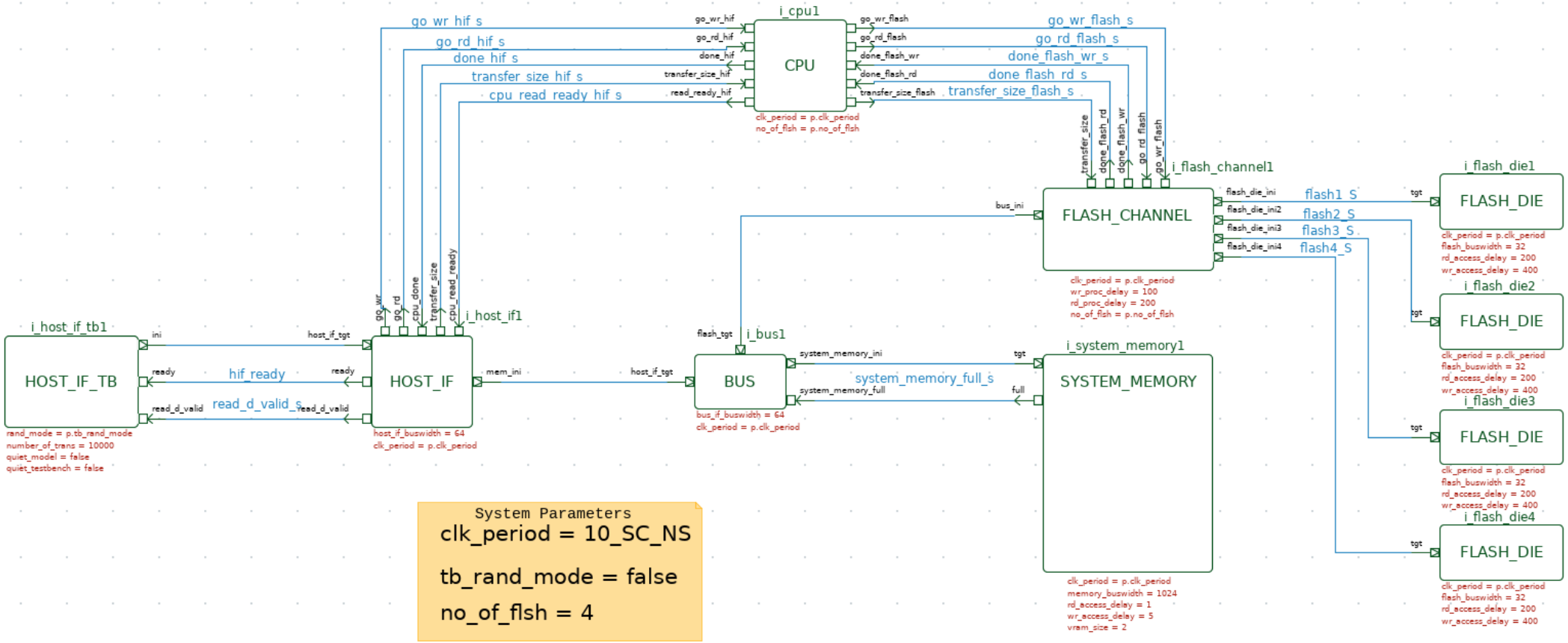
Modelling Approach in Coside



System Parameters

clk_period = 10_SC_NS

tb_rand_mode = false

no_of_flsh = 4

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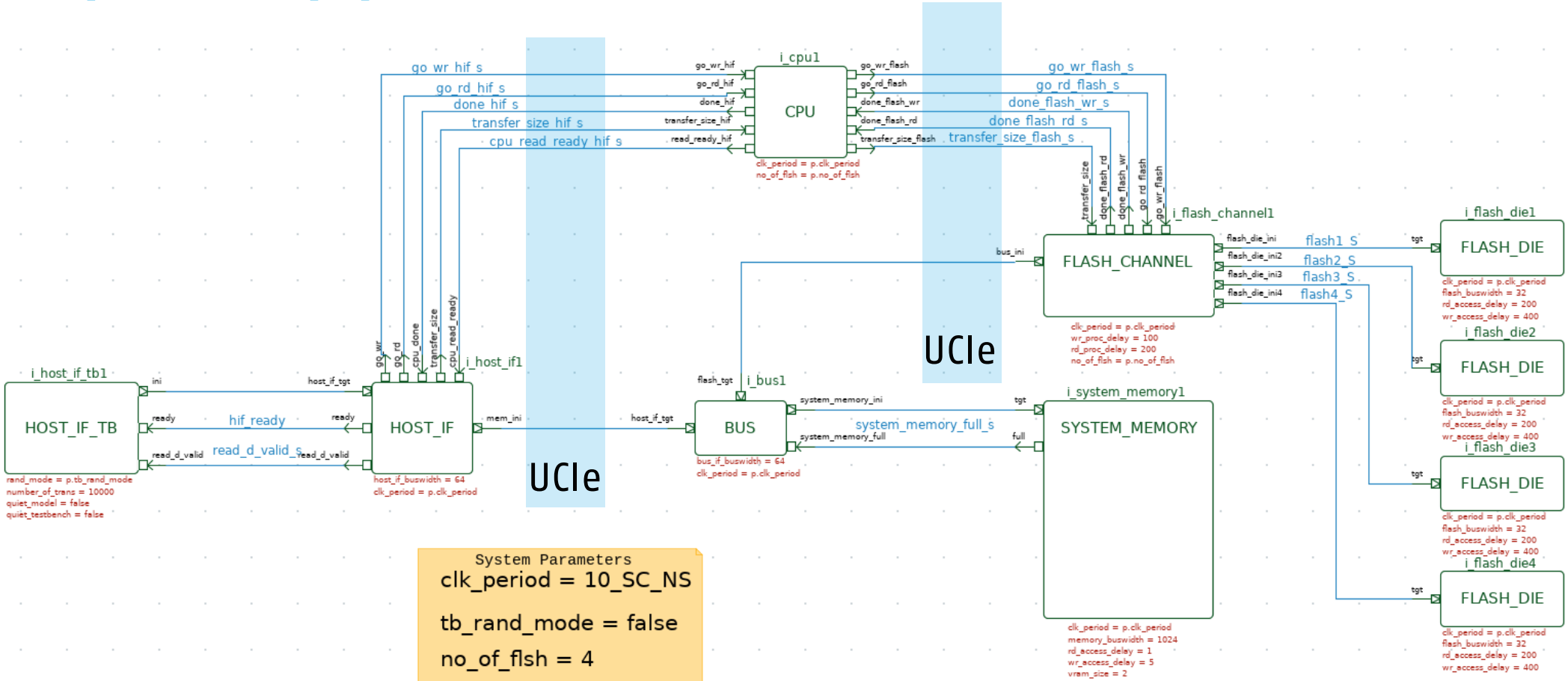
Chiplet Approach in Coside



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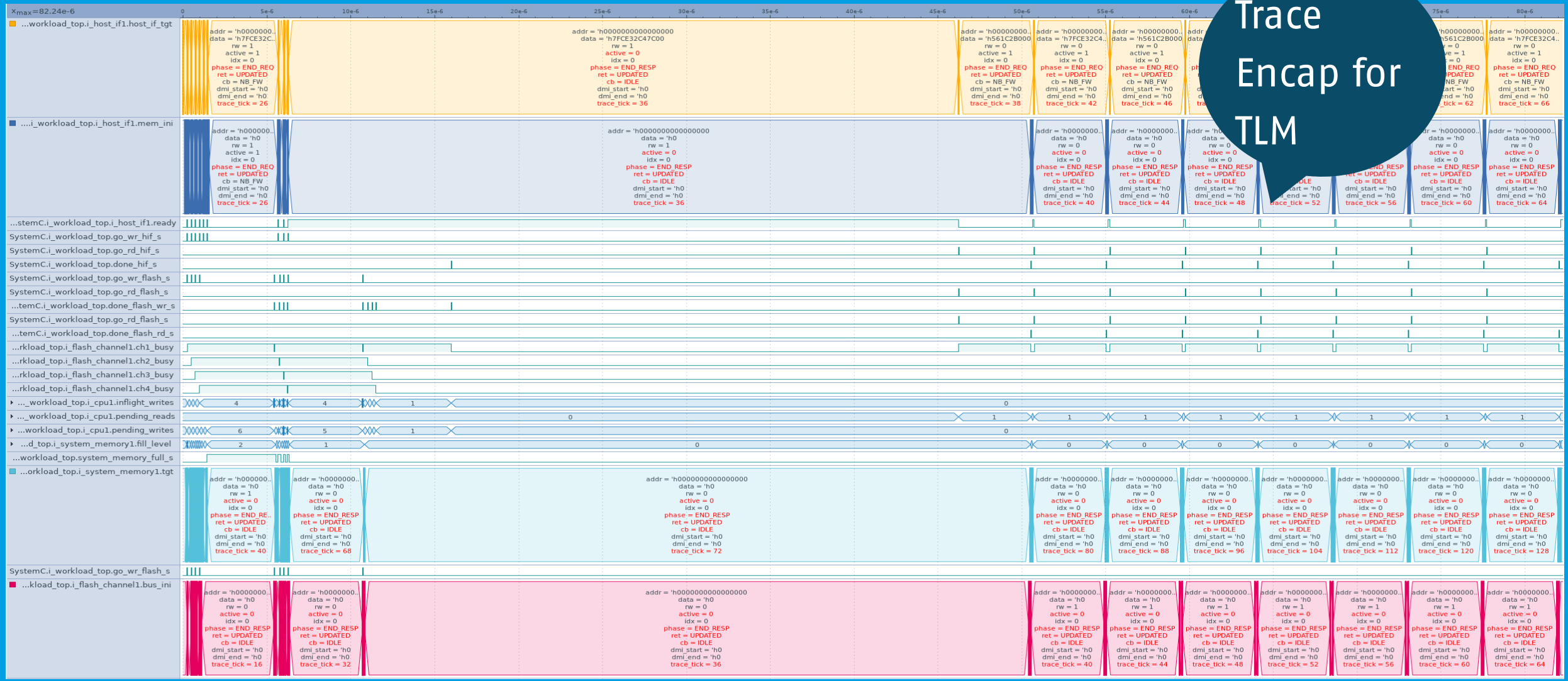
Detailed TLM/Signal Tracing



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Q & A

Any Questions?

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System Integration Excellence

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