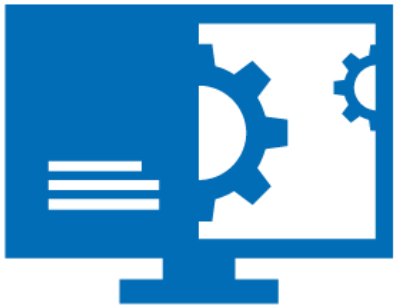
KÄRNTEN
University of Applied Sciences



COSIDE® as Key Enabler to Introduce IEEE1666.1 SystemC AMS in Education with Focus on Chip Design at FH Kärnten

25.11.2022, Wolfgang Scherr

CARINTHIA INSTITUTE FOR MICROELECTRONICS

www.cime.at

Content

- Introduction of FH Kärnten / Carinthia University of Applied Sciences and the Carinthia Institute for Microelectronics
- The “Integrated Systems and Circuit Design” Master Study Program: the influence of modern standards/tools like IEEE1666/Coside
- Using SystemC AMS for Teaching: Why it is useful - plus some examples from lectures and the student project

Carinthia University of Applied Sciences (CUAS)

- Founded in 1995
- Budget in 2021: € 42 Mio.
- Research volume: 6,5 Mio €
- Staff
  - 435 professors & full-time lecturers, central services
  - 500 adjunct faculty per semester
- Students
  - 2500 students
  - 10% international students
  - 1100 students at Campus Villach

KÄRNTEN Forschungsgesellschaft
EMV - MESS- UND PRÜFLABOR

EMC - measuring and testing laboratory

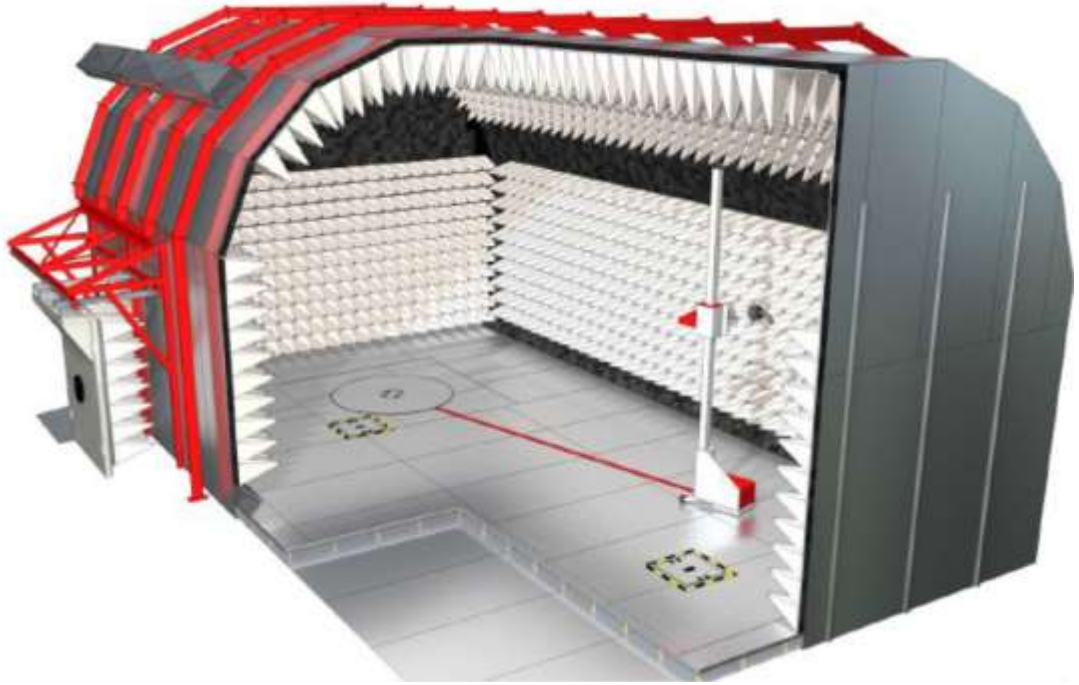
State accredited testing laboratory No. 185 for electromagnetic compatibility

ISO EN 17025:2017

- 2014/30/EU EMC Directive
- EN 60601-1-2 Medical electrical equipment (EMC)
- EN 301489 - x ETSI Series for EMC Standards (RED)
- EN 62233 EMF measurements

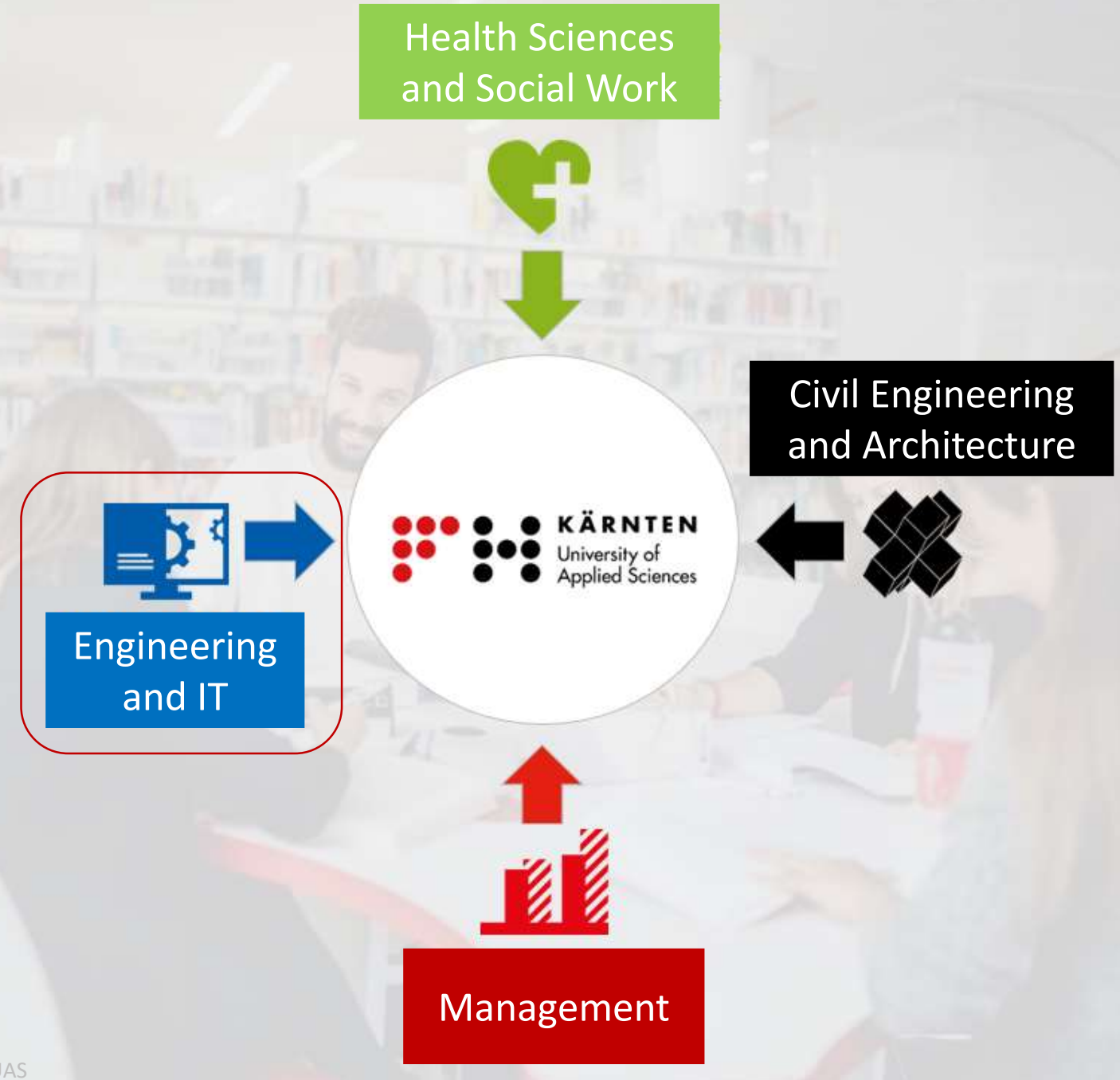
Status 2022:

- Newly built modern laboratory building with 600 m² laboratory space
- 51 accredited measurement and test methods



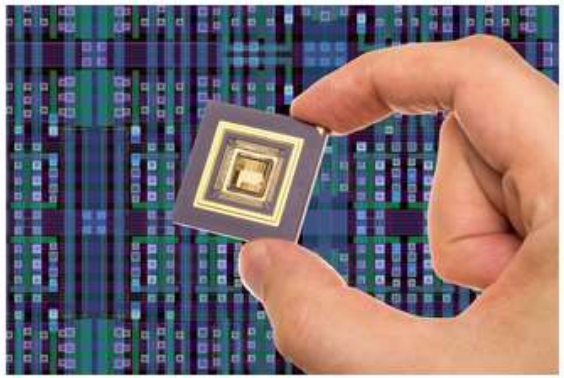
Semi absorber hall SAC 5m
- CISPR 16-1-4 (NSA, SVSWR)
- IEC EN 61000-4-3 (FU)
- CISPR 25, ISO 11452
- FCC ANSI C63.4

Full absorber hall FAR 3m
2 pcs. shielding cabins
Emission measuring stations
…



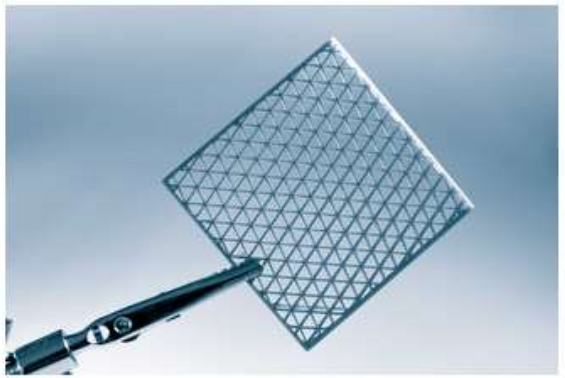
- Study programs accredited through AQ Austria:
  - 19 Bachelor and 19 Master Degree Programs
  - including 4 **Double Degree Programs** with partners in Finnland, Germany and Italy
  - including 7 master and 1 bachelor degree programs **taught completely in English**
- Planned also:
  - European Master on Active Ageing and Age-friendly Society
  - Bachelor in Technologies for Environment and Climate Protection

Research Centers @ CUAS



CIME

Carinthia Institute for Microelectronics



CiSMAT

Carinthia Institute for Smart Materials

IARA

Das Institute for Applied Research on Ageing (IARA) erforscht die Herausforderungen und Potentiale einer älter werdenden Gesellschaft.

ADMiRE

Additive Manufacturing, intelligent Robotics, Sensors and Engineering

Carinthia Institute for Microelectronics (CIME)

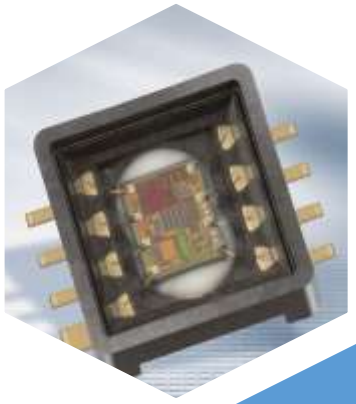
The **Carinthia Institute for Microelectronics** is a pool of experts with the clear passion for leading edge integrated circuit design.

We are a diverse team consisting of young talents, engineers, Post-Doc scientists and "old hands" with decades of industry experience.

Our research focus is on design and modelling of integrated circuits for different fields of applications like integrated sensors or wire-less and wire-line high speed communications.

Dr. Johannes Sturm

Head of Carinthia Institute
for Microelectronics

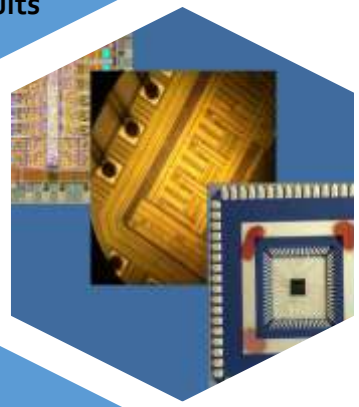


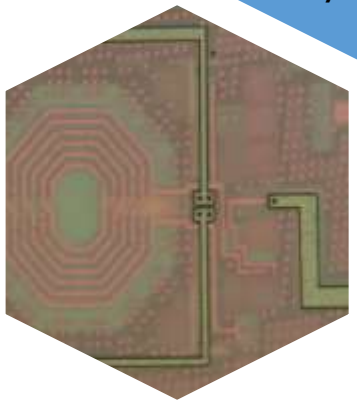
RESPECT

Research group for Modelling and Design of Integrated Systems and Circuits

SIMS

Research group for Sensor Integration in Mechatronic Systems





RFFE-Lab

Research Lab for Radio Frequency Frontends

Key facts (2021):

Staff:

- 5 Key Researcher
- 3 Senior Researcher
- 3 Researcher
- 5-10 Master/PhD Students

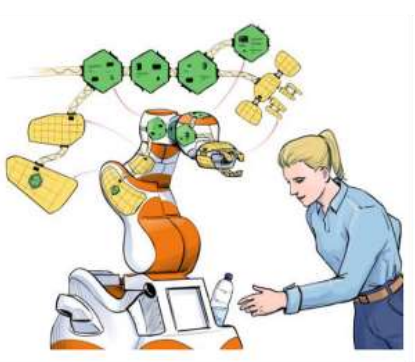
Research Projects:

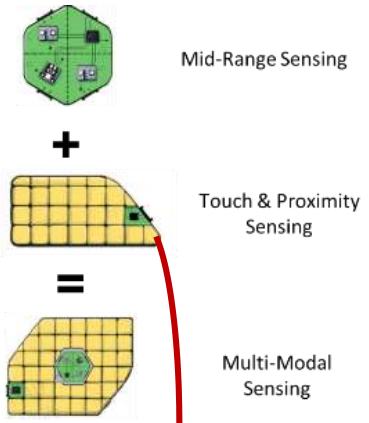
- > 600k€ / year

Project partners:

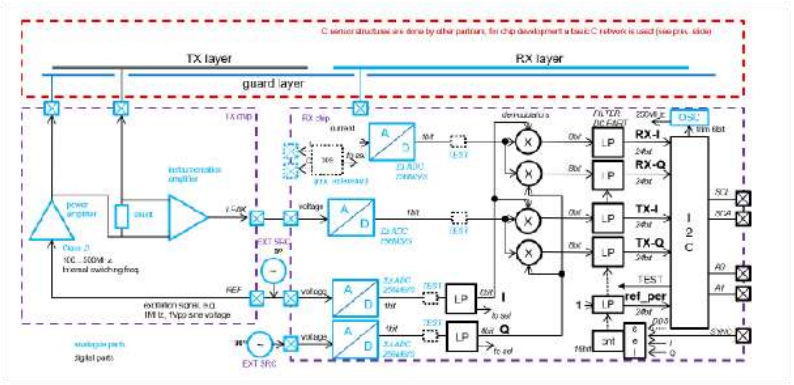
- Silicon Austria Labs
- Joanneum Research
- University of Klagenfurt
- Johannes Kepler Univ. Linz
- Infineon Technologies
- Coseda Technologies
- NXP
- CISC
- ...

Research groups and their projects:

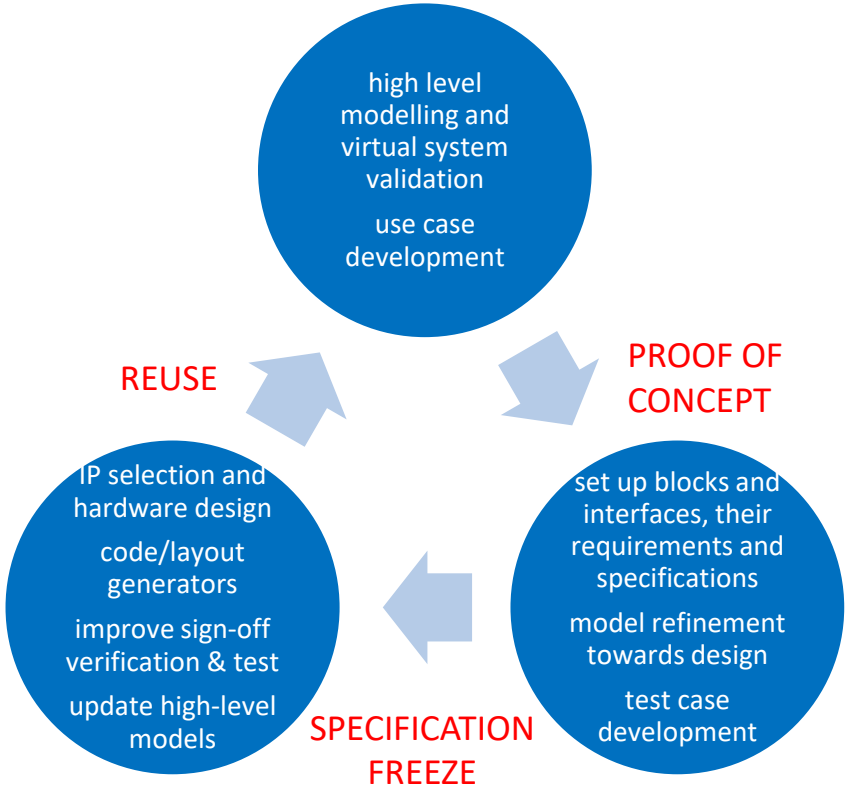


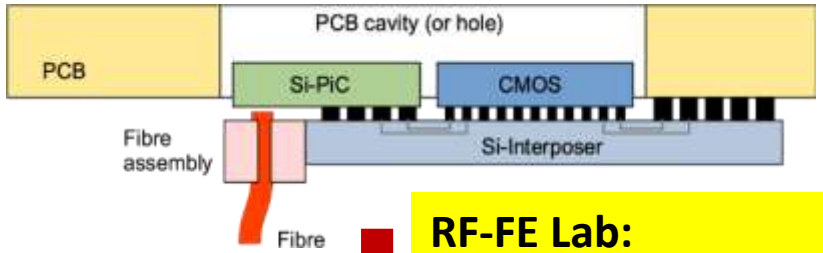


SIMS:
Perceptive Skin Sensor IC

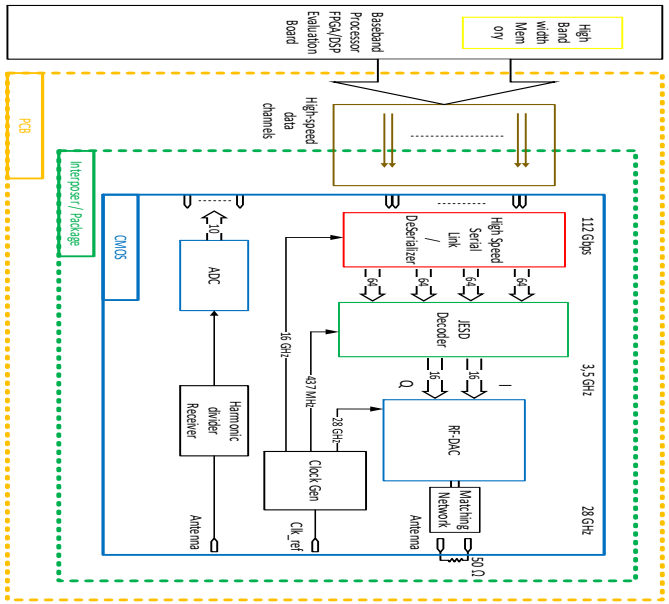


RESPECT:
Modelling and Automation



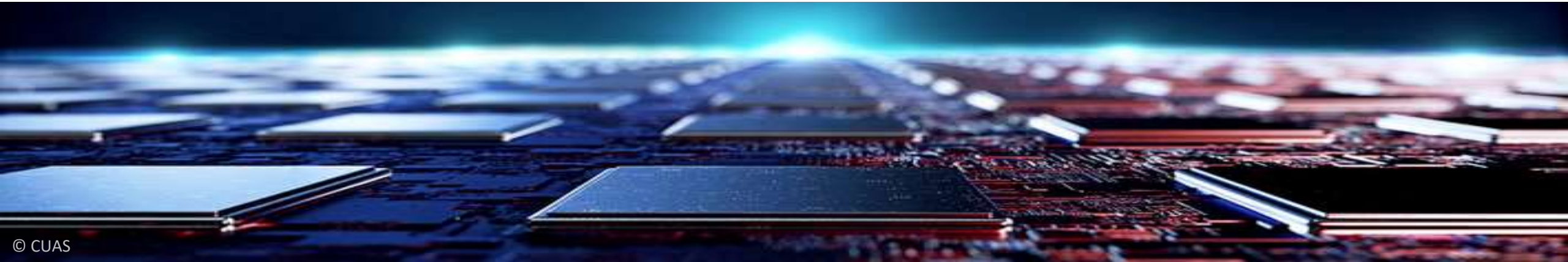


RF-FE Lab:
Photonics to RF link



Master Program - ISCD

- International master program (4 Semester, 120 ECTS, English)
- Started in 2006 (out of an electronics master program with “some” ASIC design)
- First dedicated master program on integrated circuit design in Austria
  → based on state of the art industrial tools and methodologies
- Close cooperation with microelectronic industry (guest lecturers, …)
- One of the strongest research department at CUAS
  → we regularly offer research positions for ISCD master students
  → foster academics involvement instead of “boring” standard exercises



ISCD – Job opportunities and target industry

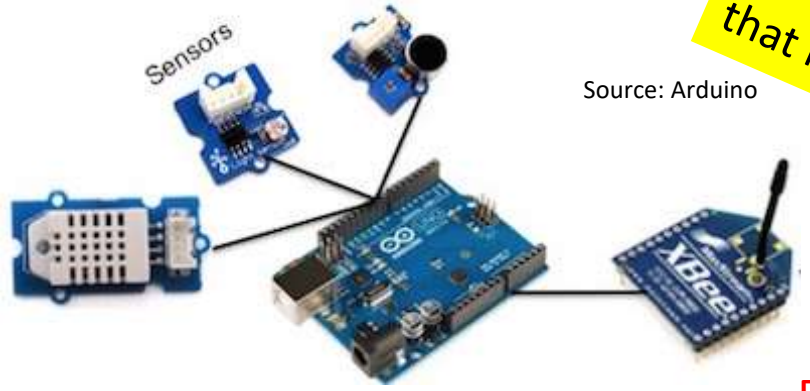
ISCD graduates can work as specialists for Austrian as well as international companies in the field of semiconductor industry (foundries, fabless foundries, and engineering companies) as well as for businesses providing electronic system solutions whose products contain highly integrated electronic components.

Their fields of activities include the

- design
- modeling
- verification
- implementation
- testing and
- technical support

of analog, digital and mixed-signal integrated circuits. Their activities also include the application support (e.g. PCB design), as well as test and product engineering.

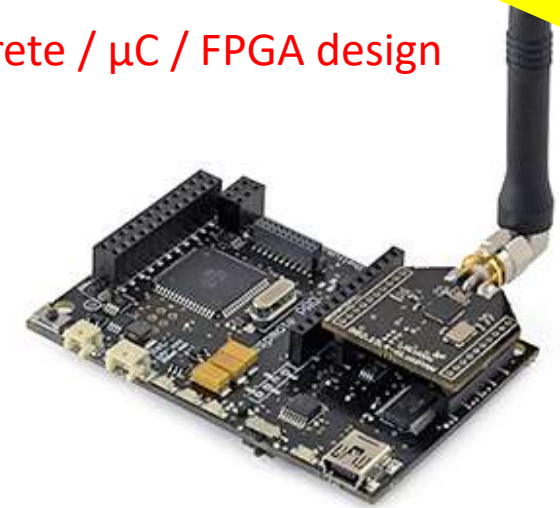
Students knowledge when starting @ISCD:



Source: Arduino

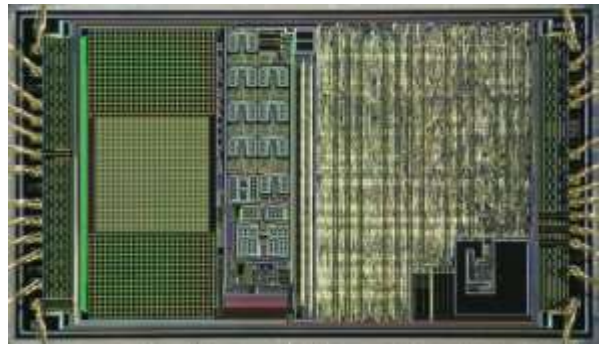
This stuff they usually know when they start the ISCD master – it is important to build on that knowledge properly…

Discrete / µC / FPGA design



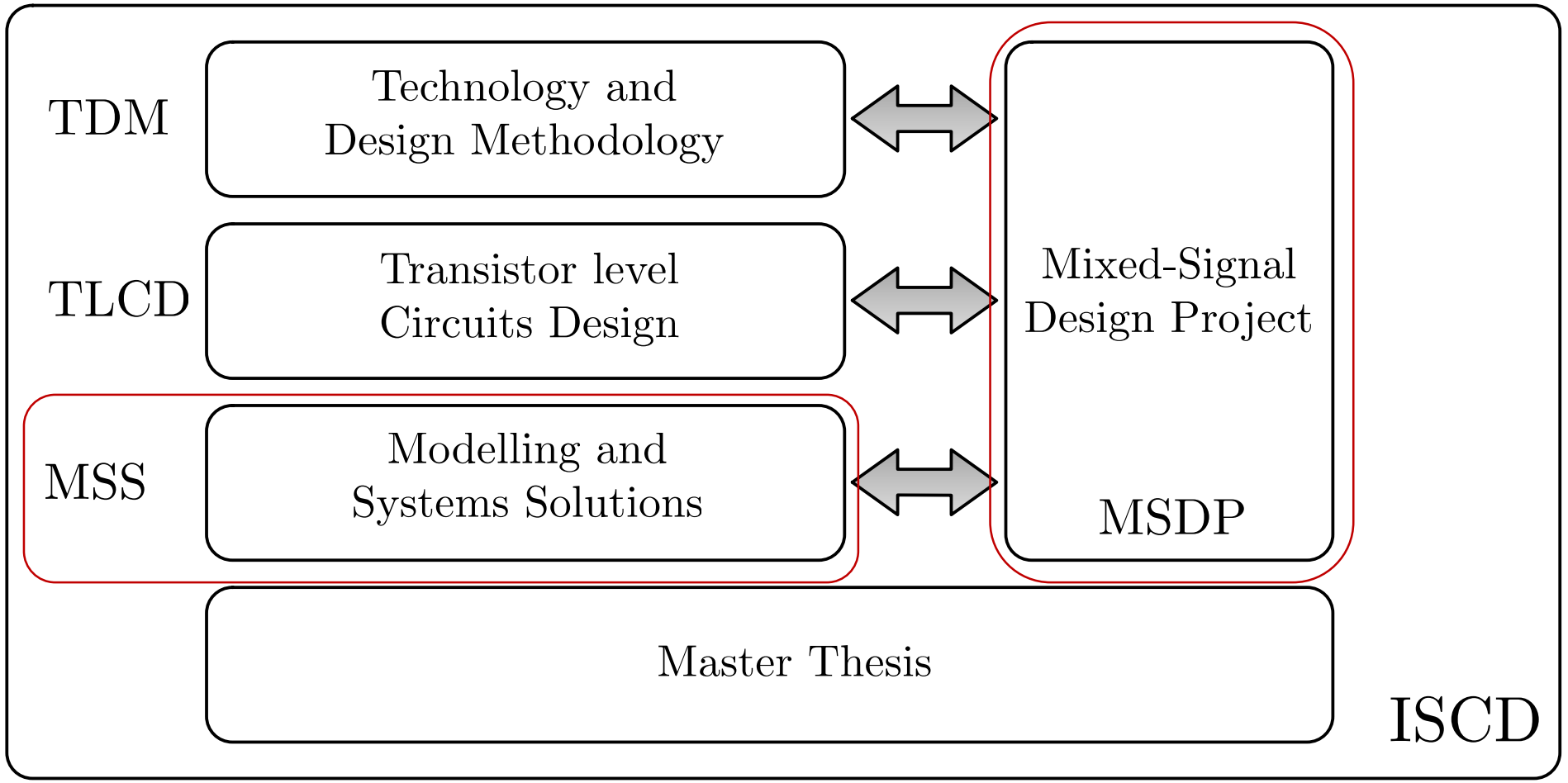
Source: Libelium, Networking - 6LoWPAN / IPv6

ASIC design



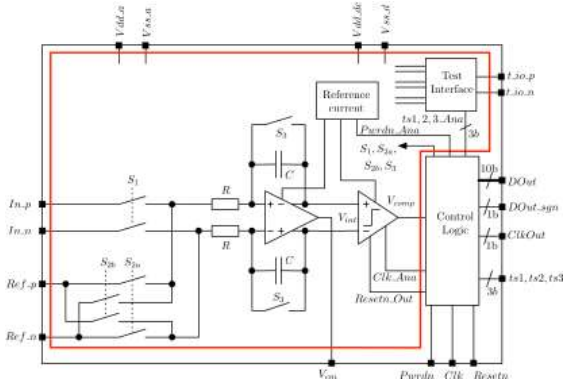
This they should learn…
…a quite new “world”.

Actual Curriculum – ISCD Master

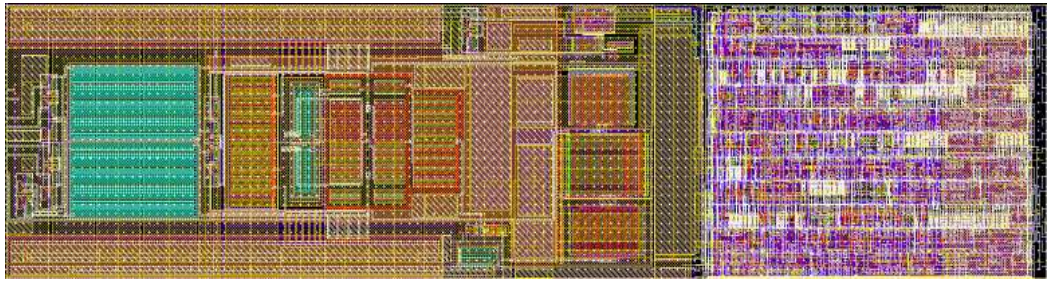


ISCD Student Project: **from Idea to Silicon** (unique for master programs!)

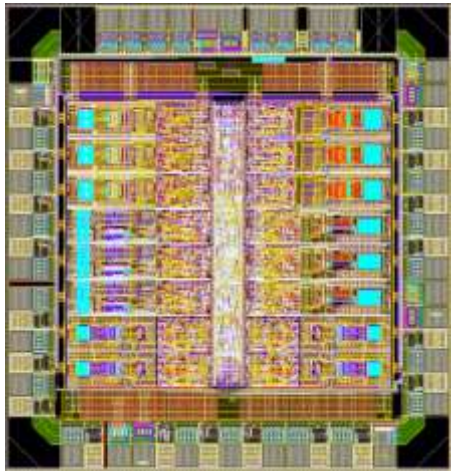
Analog and digital circuit design



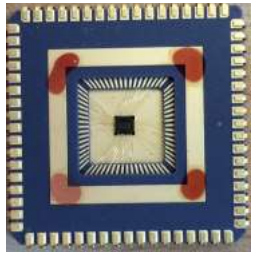
IADC top-level layout



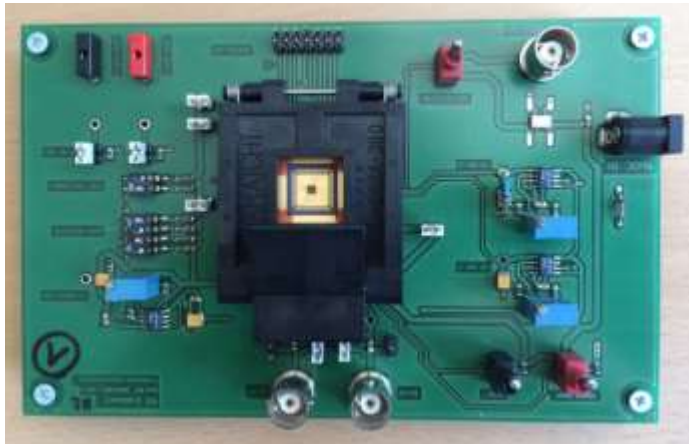
Analog Frontend — Digital Logic



Testchip top-level layout



Testchip production and packaging



Lab evaluation board

Technology also involves in education, requiring also more modern methodologies…

CMOS 0.35µm

2006

CMOS 180nm

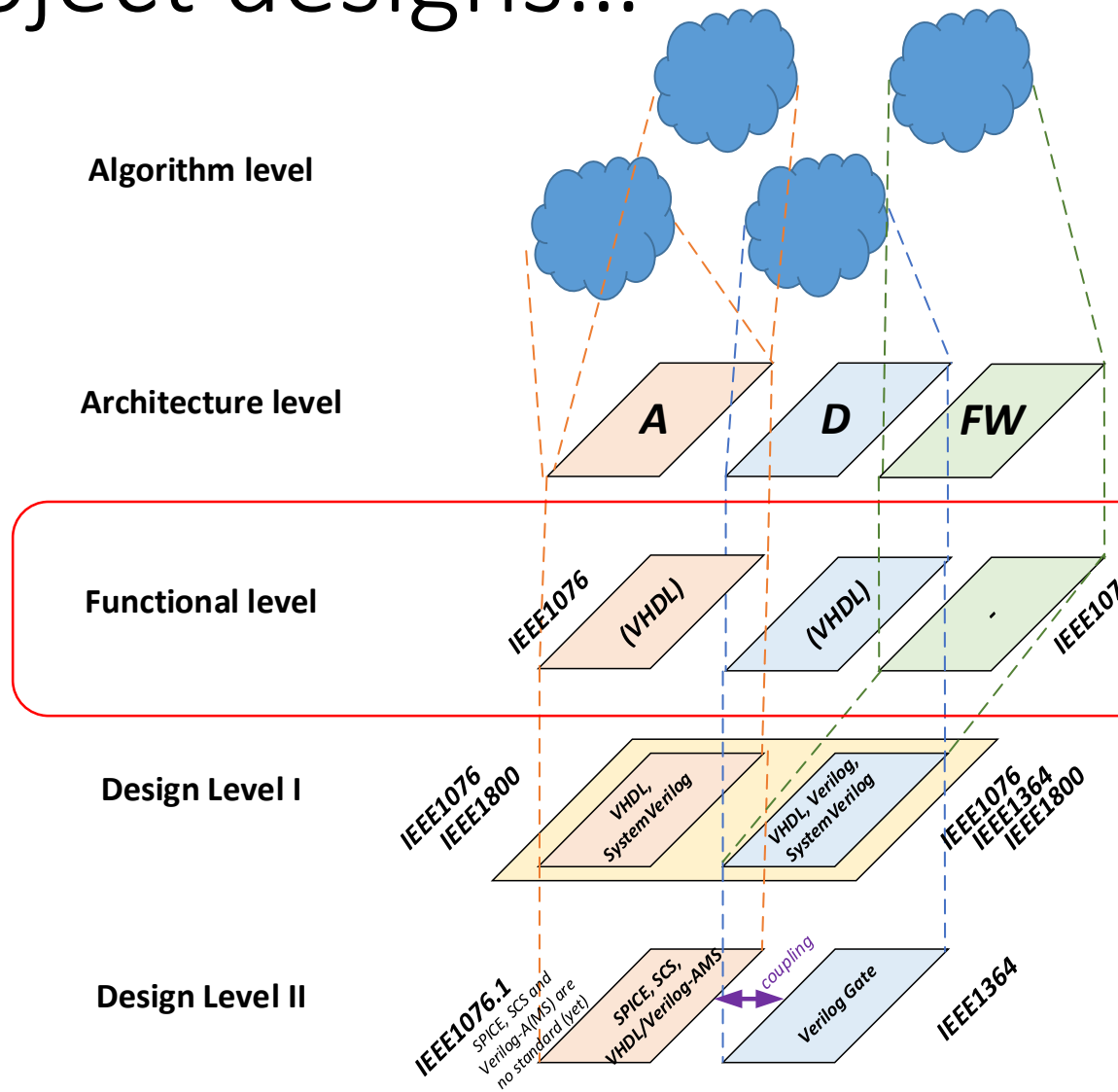
actual target for
the student project

CMOS 65nm

EUROPRACTICE

2022

“old” ISCD setup for lecturing and research project designs…



Matlab, Simulink

C/C++

Office Tools

The functional level showed quite some gaps…

Paper & Pencil

Modelsim

Virtuoso, ADE, Spectre, …

Design Compiler, Formality, PrimePower, …

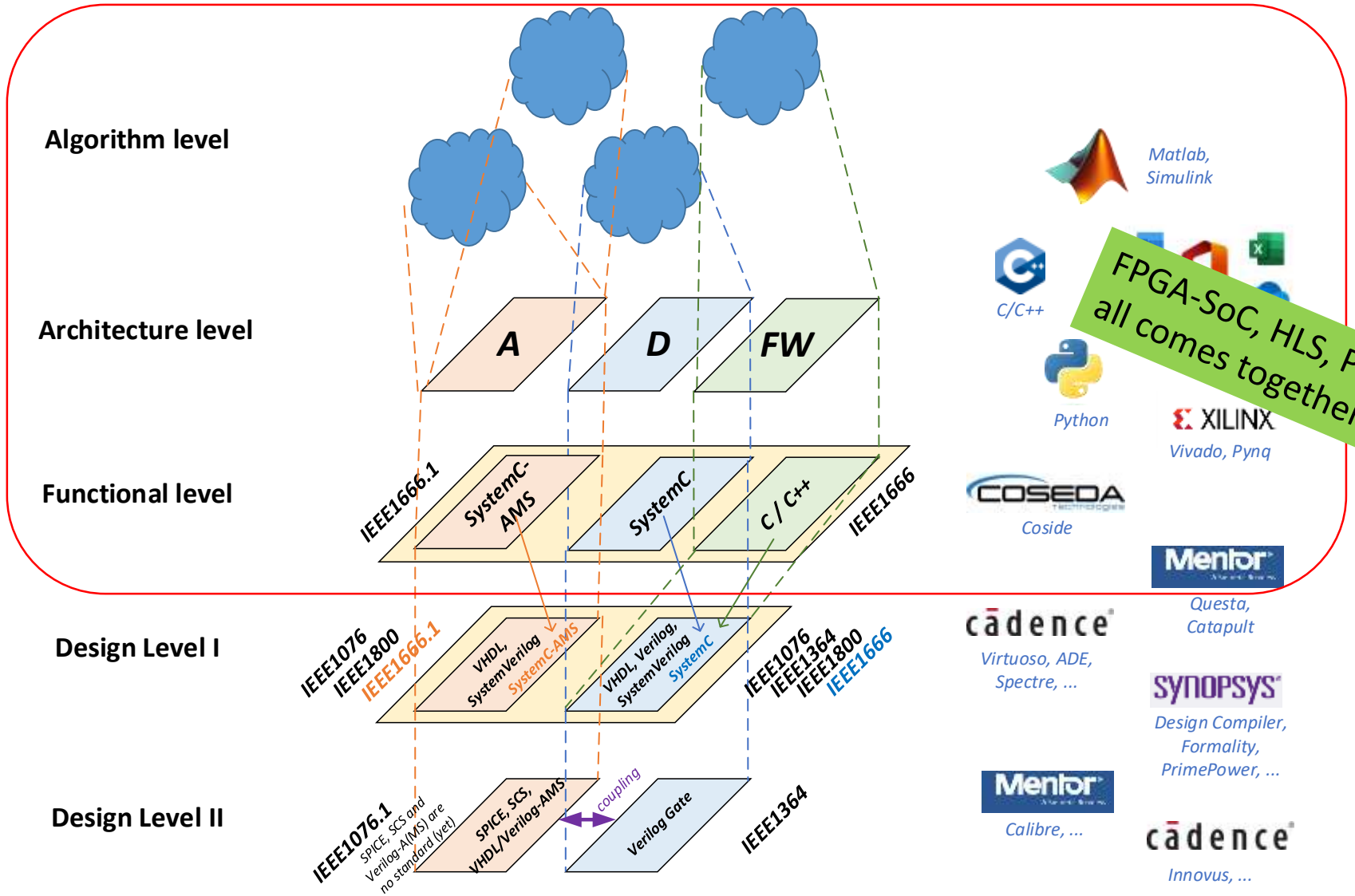
Calibre, …

Innovus, …

…these are important links to “existing” knowledge!

… and after Coside® was introduced

(for the actual curriculum)



Matlab, Simulink

C/C++

Python

XILINX
Vivado, Pynq

COSEDA
Coside

Mentor
Questa, Catapult

cadence
Virtuoso, ADE, Spectre, …

SYNOPSYS
Design Compiler, Formality, PrimePower, …

Mentor
Calibre, …

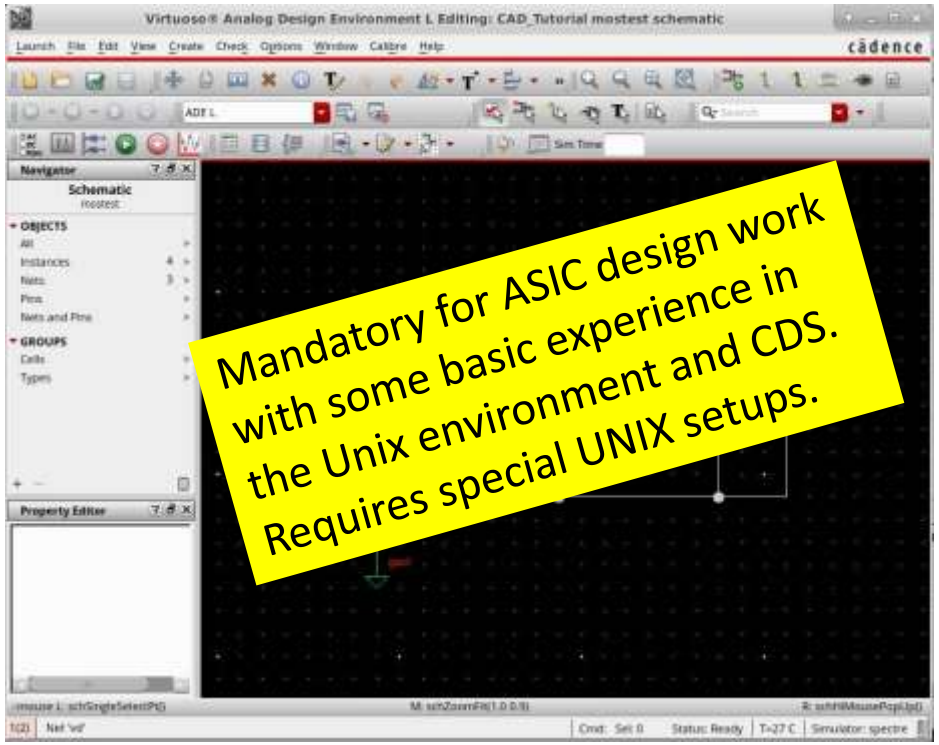
cadence
Innovus, …

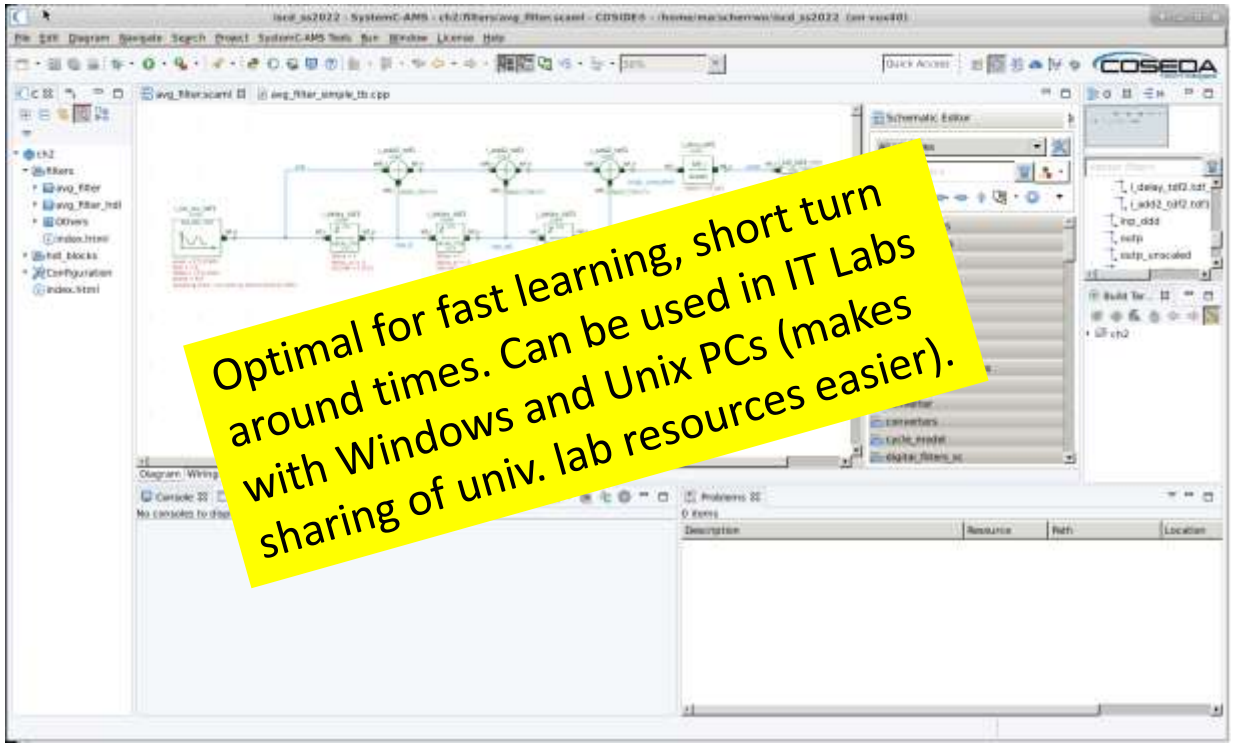
FPGA-SoC, HLS, Python, Matlab/Octave, … all comes together with a low entry barrier!

Mixed-Signal modelling revived…
→ low entry level for beginners

- Good for just **analogue** ASIC design /w some experience
- Min. 8x3h sessions + 4 labs to learn its initial usage
- Basic (analogue) library, no useful digital/system libraries
- No graphical representation for digital design

- System level tool with options to go down to a basic design level
- Easy to learn for students in 1,5x3h sessions + 2 labs
- Extensive set of prebuilt **analogue and digital** libraries to start with
- Digital design also using schematics (e.g. with DE and TDF)





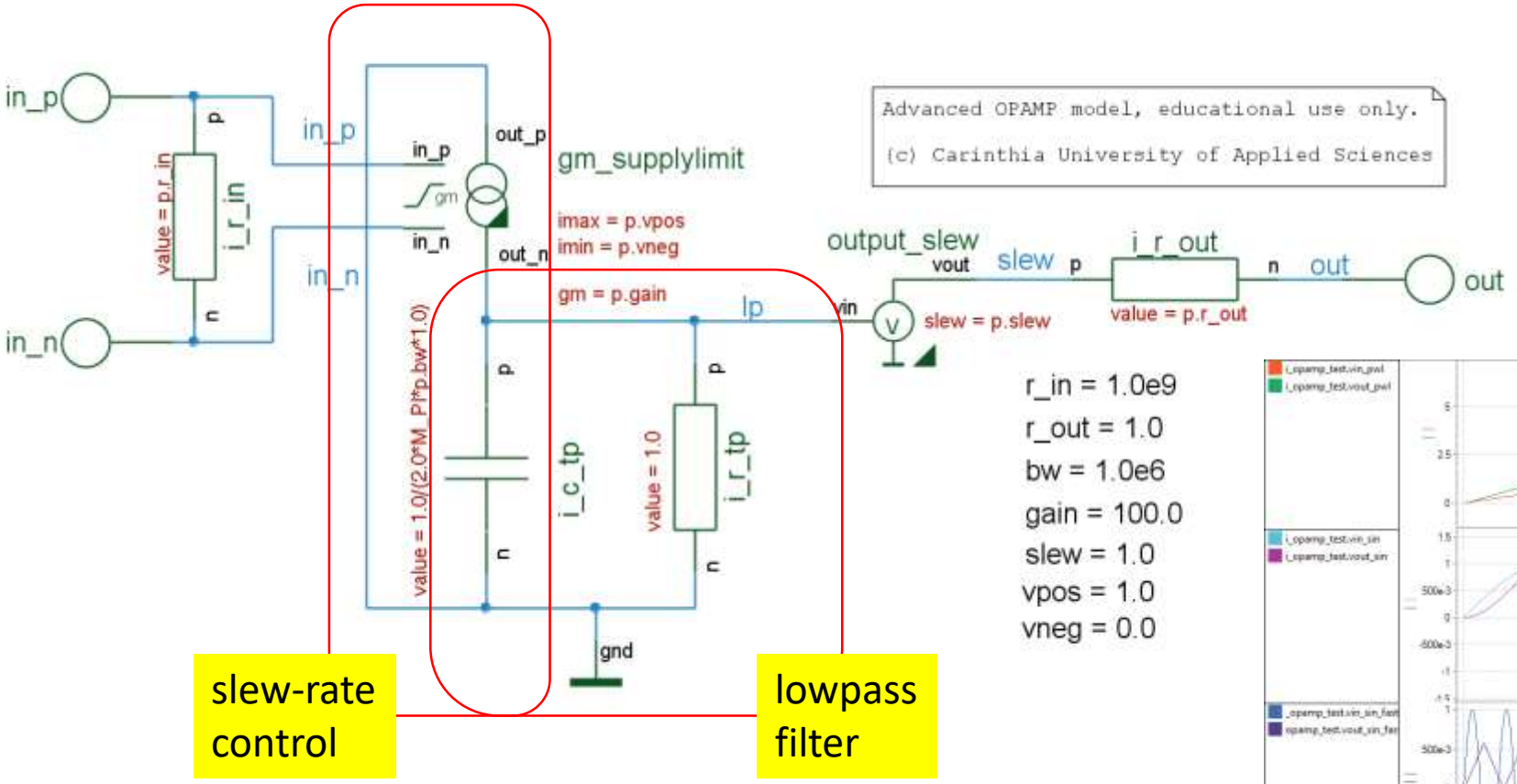
Learning analog macro modelling with Coside®

- Look-and-feel similar to Windows tools, so low entry barrier for students (they often worked with Simulink and Vivado on PCs before)

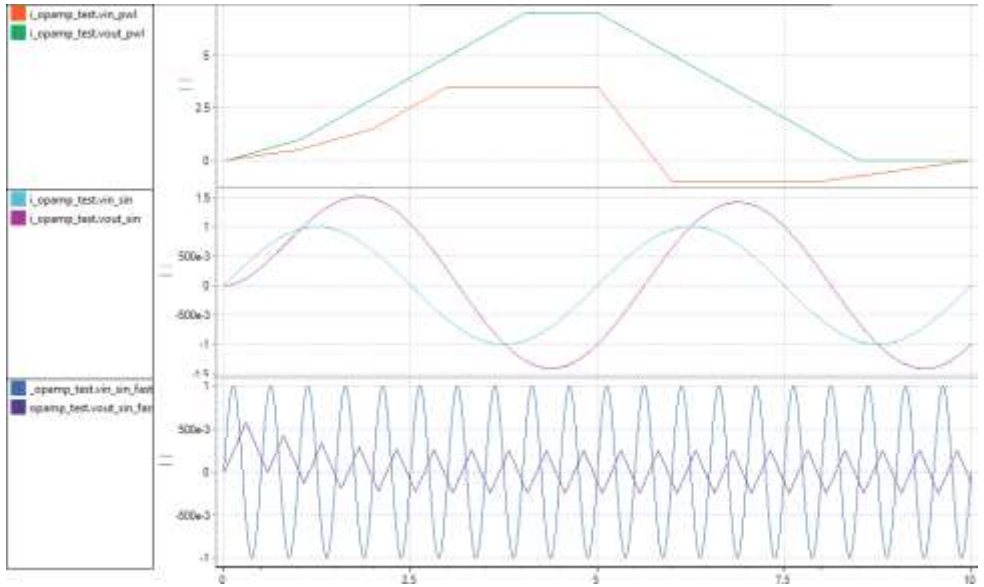
- Students don’t need to learn a language first, they can start with simple models on visual level and learn any HDLs afterwards
  - Focus on designs and concepts instead of tools and languages

- No-fuss mixed-signal setups with ELN, LSF, TDF and DE models
  - In comparison, in an ASIC design flow it needs a coupling of SPICE + digital simulator + Simulink to do something similar, such a setup is by far non-trivial !

Modelling examples: **Band-limited and slew-rate limited OPAMP**

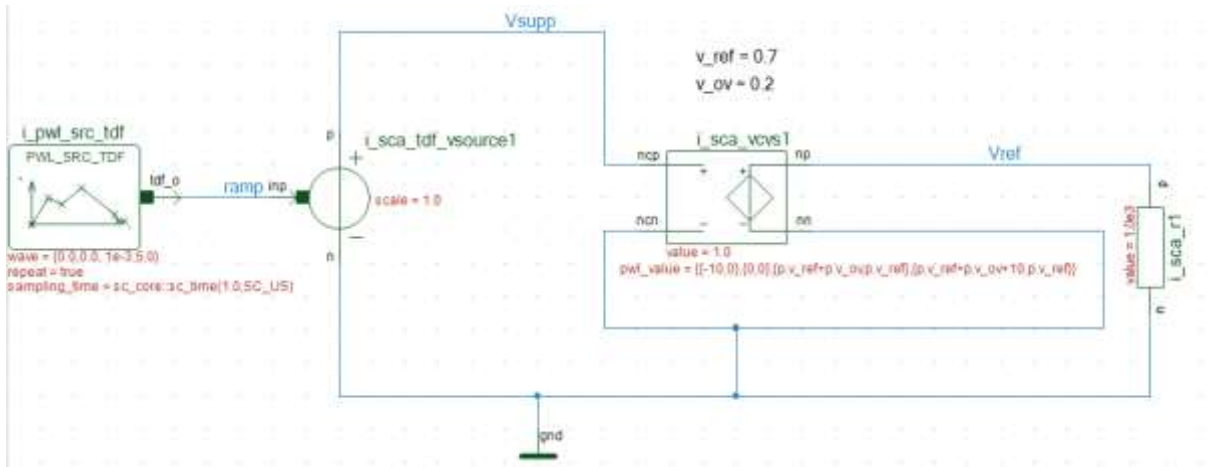


r_in = 1.0e9
r_out = 1.0
bw = 1.0e6
gain = 100.0
slew = 1.0
vpos = 1.0
vneg = 0.0

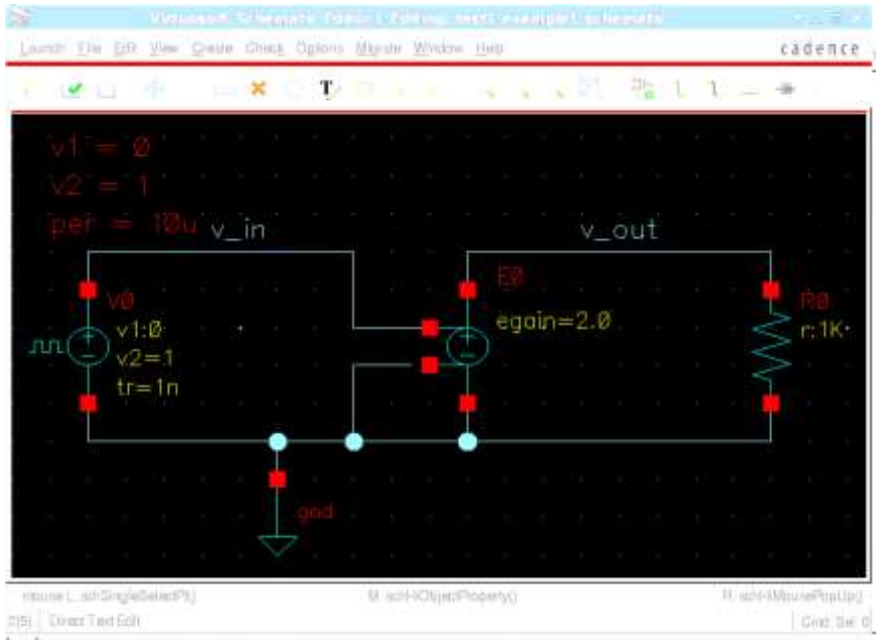


Not to forget: easy transition of new knowledge to an ASIC design flow/tool!

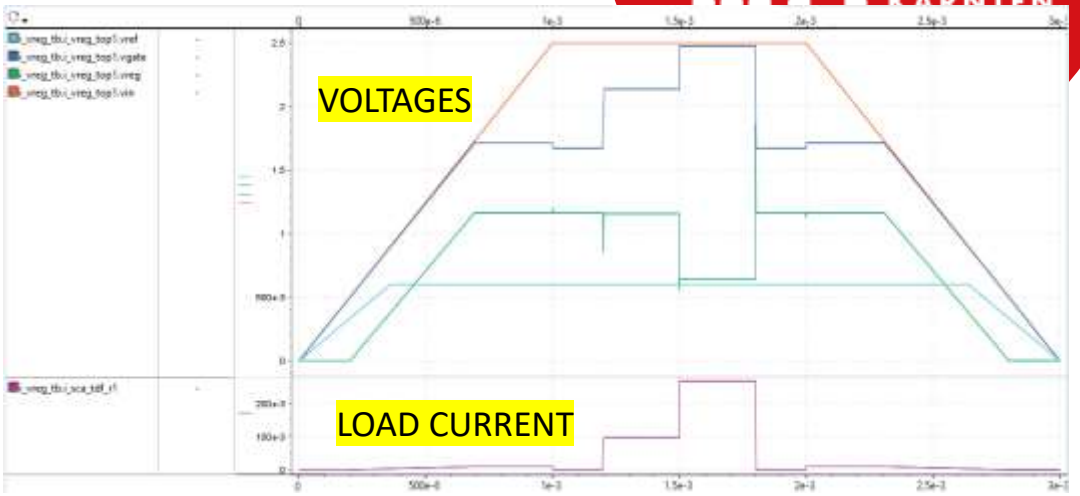
Coside ELN model



Spectre analog model



Typical student lab (ELN): a simple voltage regulator



Device model (PWL table model)
if vg>vt: Id = gm * (vg – vt) ,
otherwise: Id = 0
(optional: go for a simplified square-law MOS model)

Ramp from 0V to 2.5V to 0V

Vin

TESTBENCH: "real" voltage source

buffer cap

Pass Device

gm, vt

Vout

1.2V
0mA to 100mA,
ramps, pulses, …

TESTBENCH: "real" load scenarios

vg

diff.-amp

bw

DIFF

gain

+ -

Clamp to input supply!

Clamp to input supply!

Reference

Vref

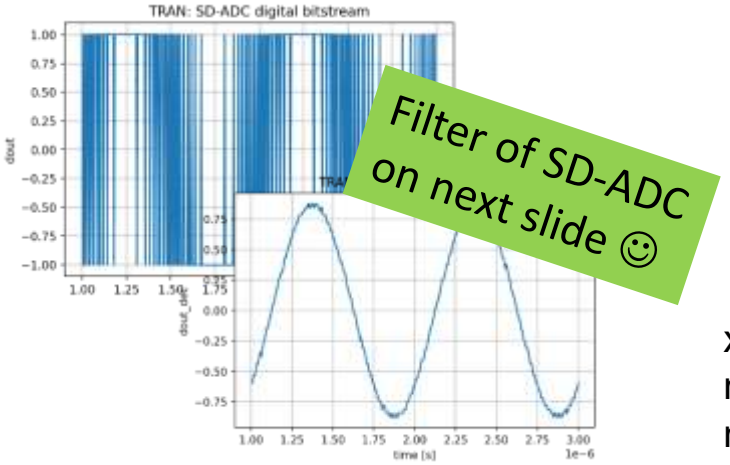
impedance of sense

Sense Device

buffer cap

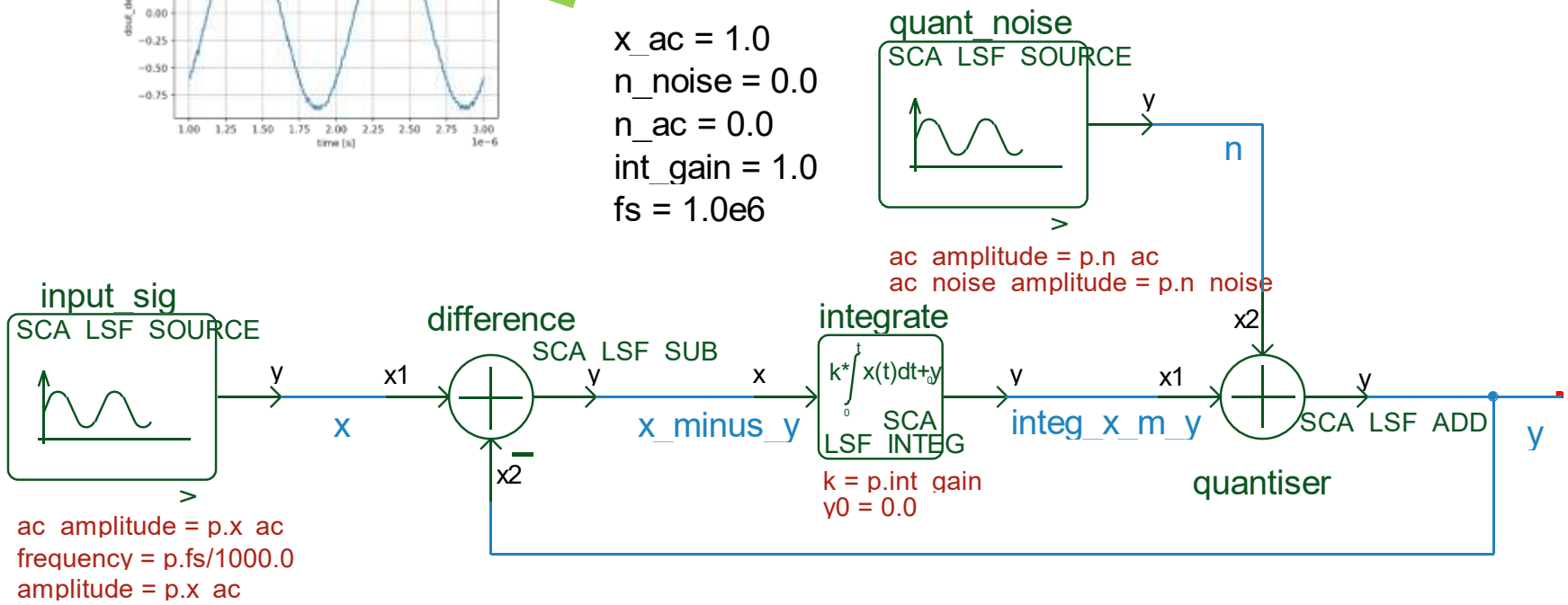
(optional: optimise gain and BW or define an improved regulation loop by oneself)

LSF modelling for learning ADC concepts…

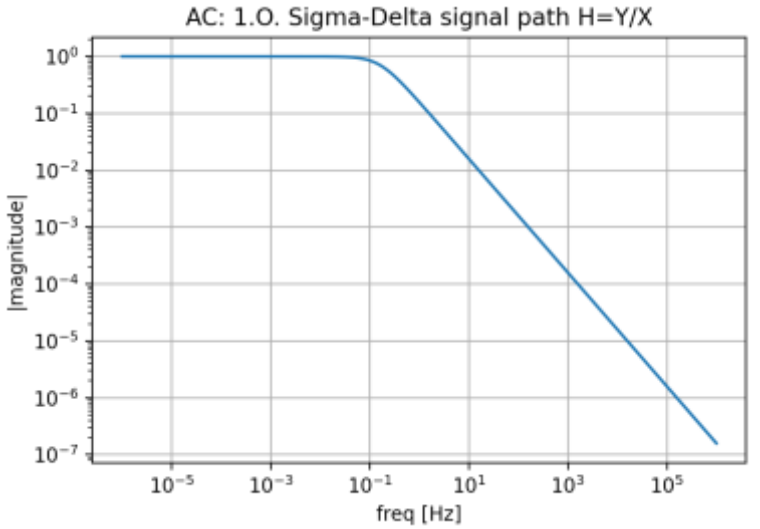


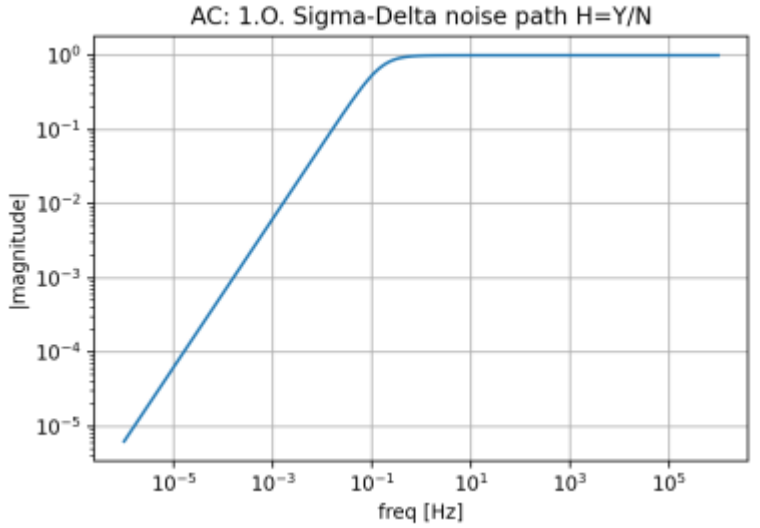
Filter of SD-ADC on next slide ☺

x_ac = 1.0
n_noise = 0.0
n_ac = 0.0
int_gain = 1.0
fs = 1.0e6

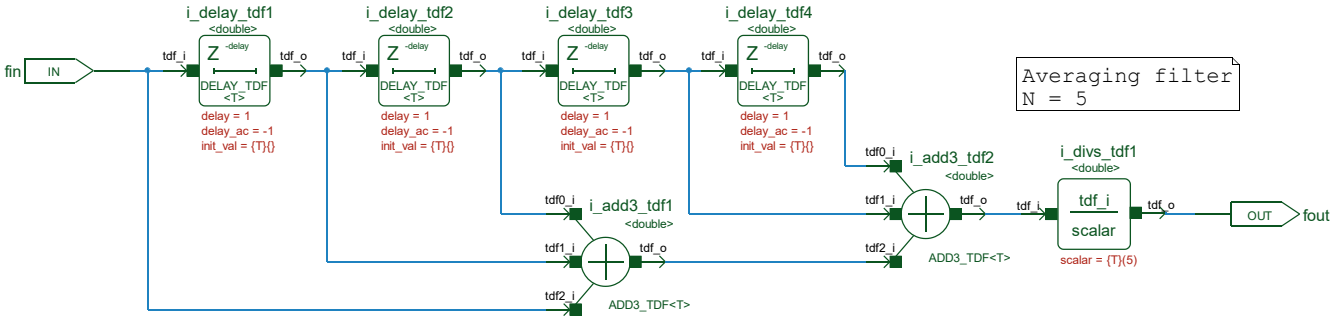



```
input_sig -> set_timestep(1.0/p.fs, sc_core::SC_SEC);
```

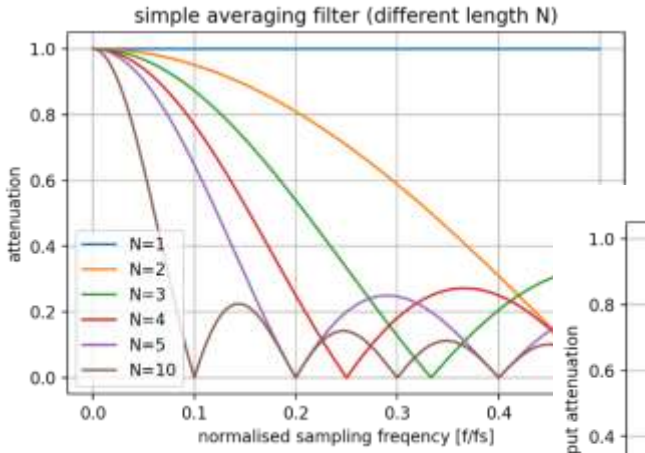




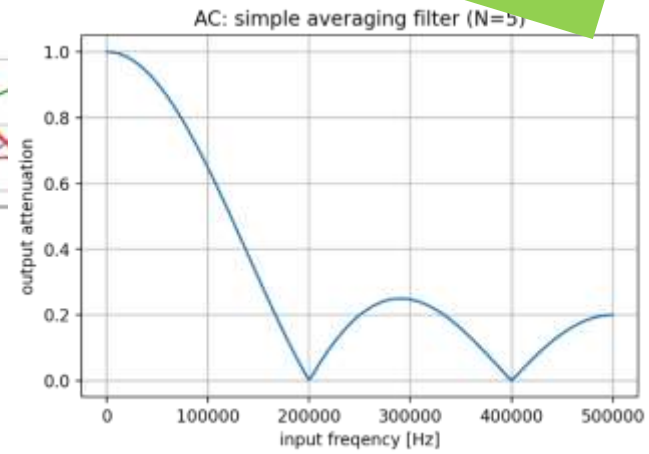
Coside® does not stop at analog modelling: e.g. learning CIC filters by exploring TDF…

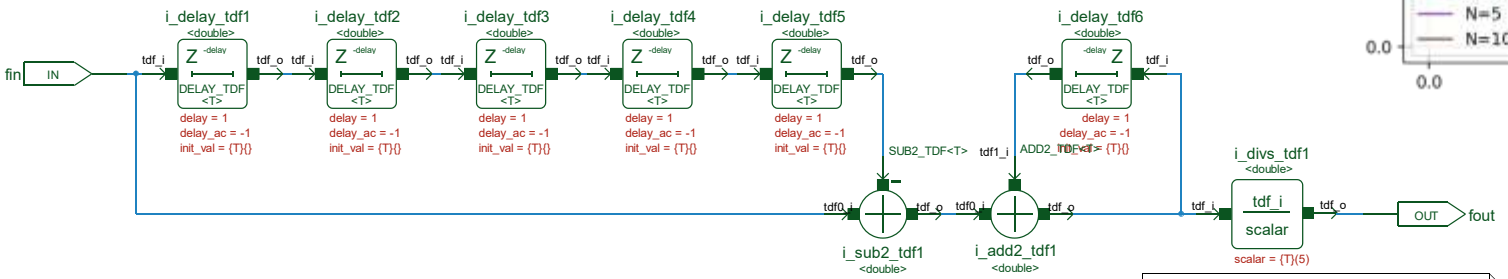


Averaging filter
N = 5



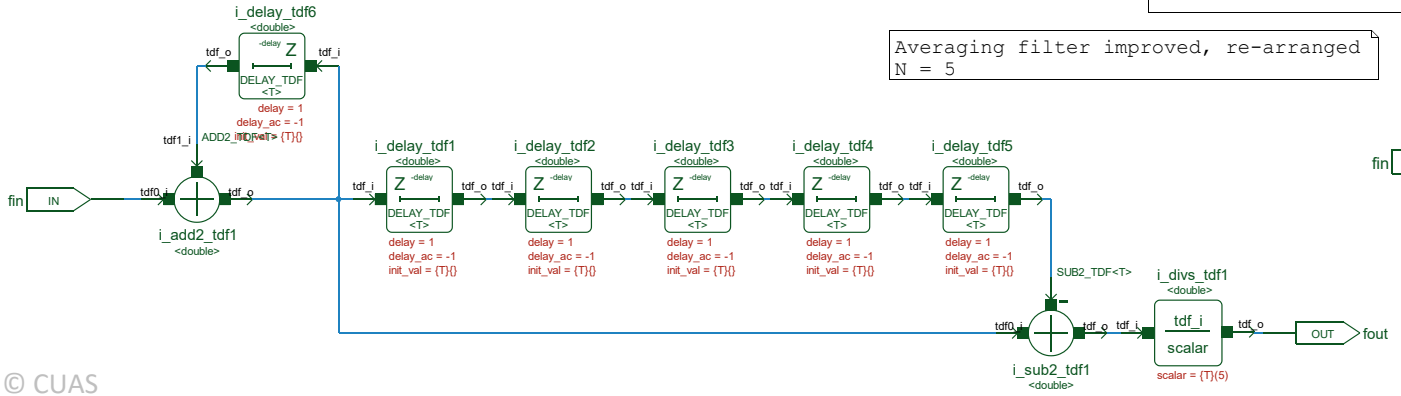
Fast AC simulation = no "FFT fuss"…

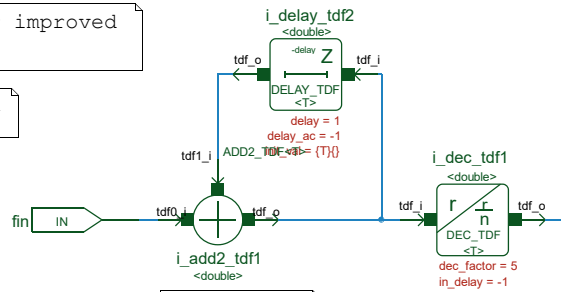


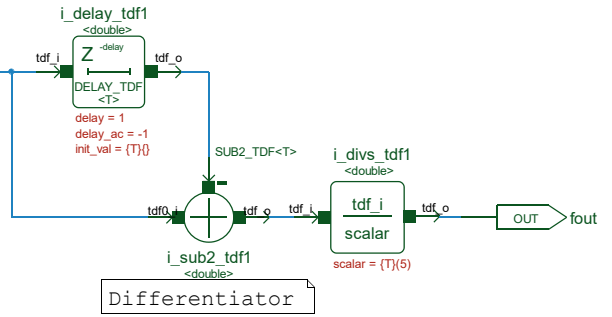


Averaging filter improved
N = 5

Averaging filter improved, re-arranged
N = 5

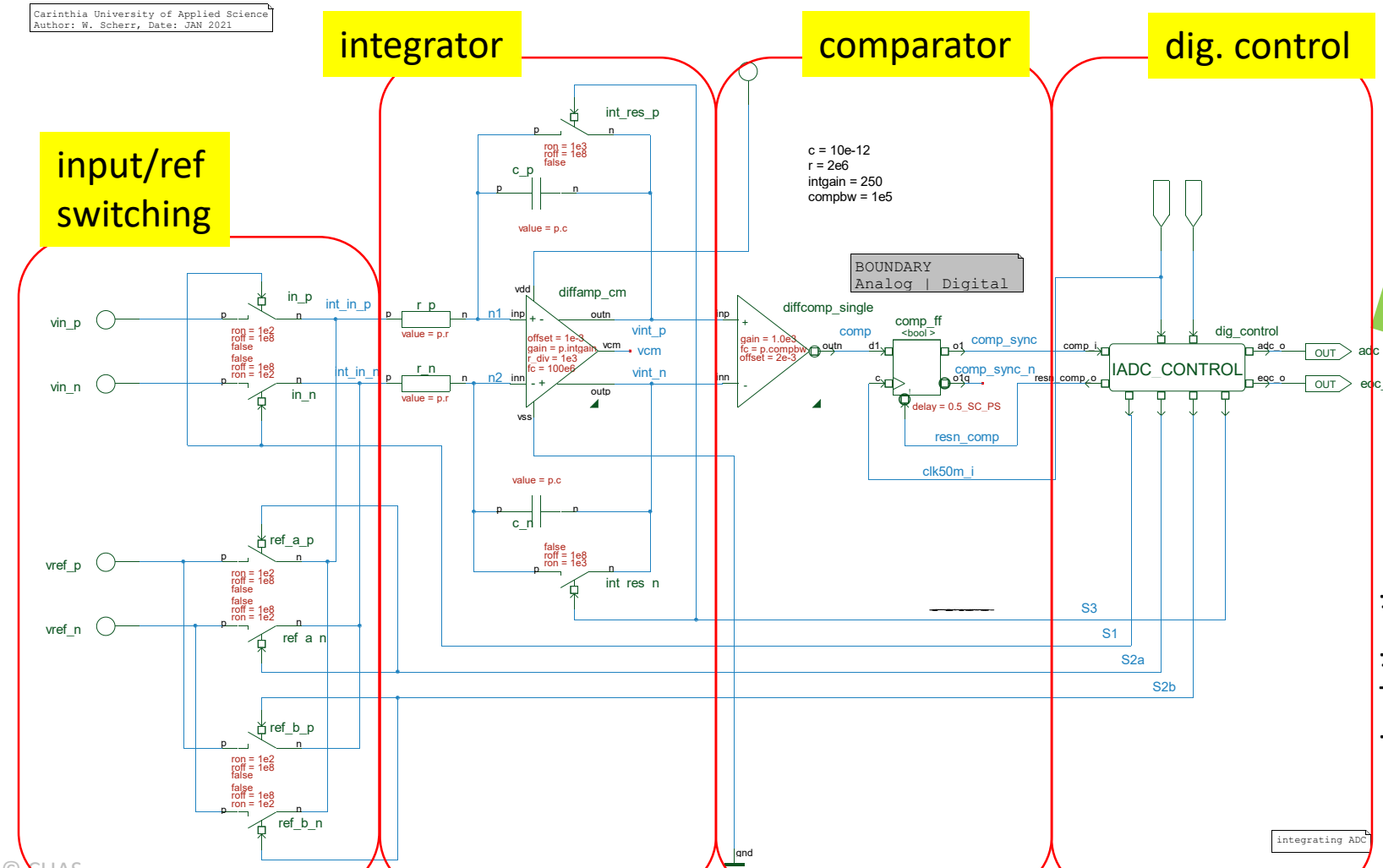


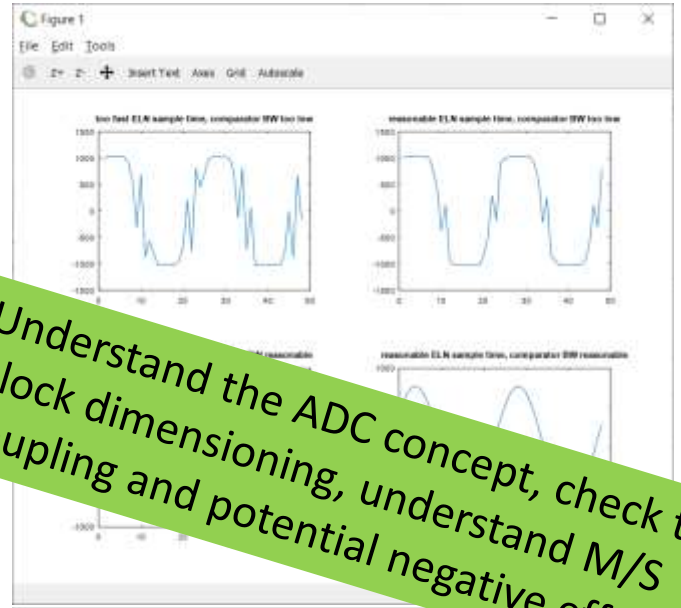




Fully optimised averaging filter --> CIC
N = 5

SystemC AMS model of the I-ADC student project – set up in a ~3h session!





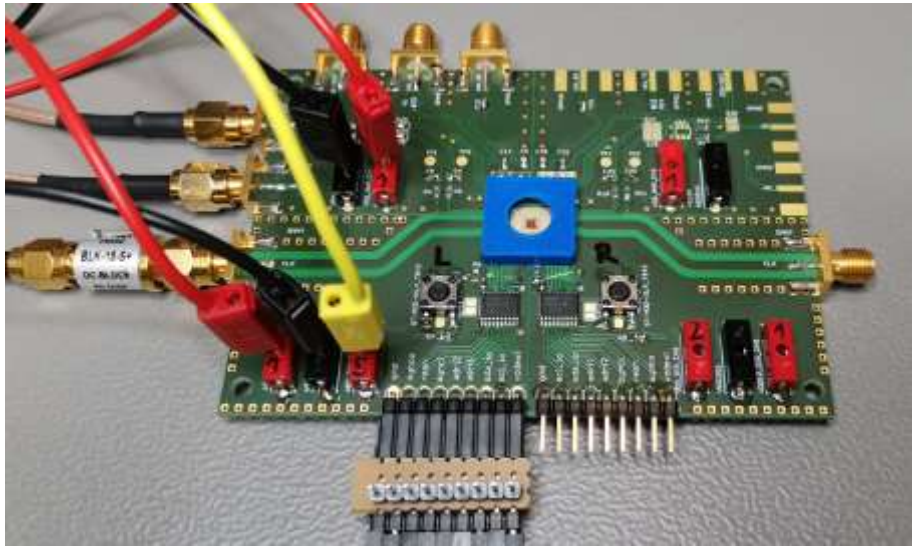
Understand the ADC concept, check the block dimensioning, understand M/S coupling and potential negative effects, ...

Student paper 2021 @ CUAS with Coside:
… finally ended up in a working test chip.

Prototyping for a DDS-based I/Q reference signal generation on a capacitive sensing chip in 65nm CMOS using SystemC AMS, C HLS and VHDL

Matthew Bio[1,2], Harald Gietler[3], Josip Plazonic[1], Manfred Ley[1], Hubert Zangl[3], and Wolfgang Scherr[1]

[1]Department of Integrated Systems and Circuit Design, Carinthia University of Applied Sciences, Villach, Austria
[2]Department of Computer Engineering, Kwame Nkrumah University of Science and Technology, Kumasi, Ghana
[3]Institute of Smart System Technologies, University of Klagenfurt, Austria



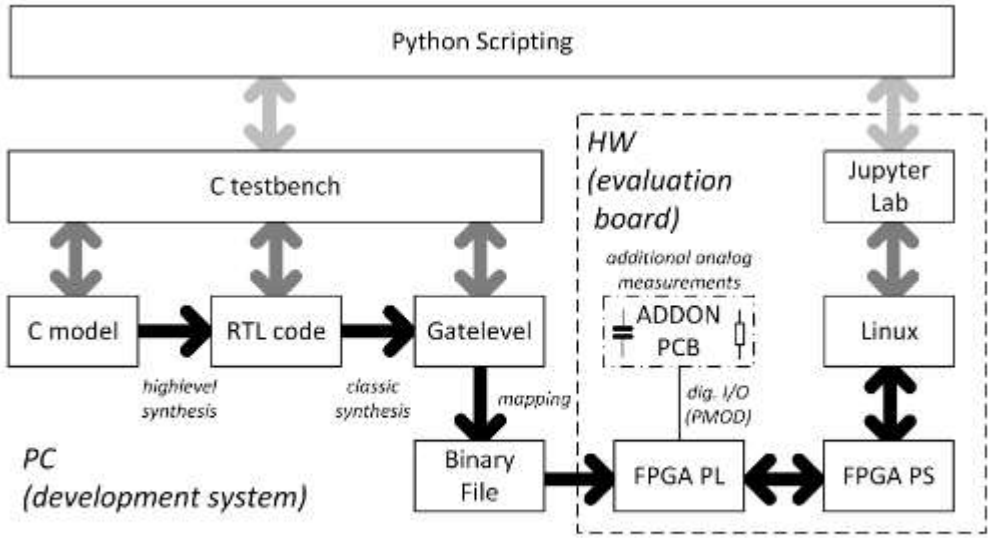


Fig. 3: Logical high-level design flow.

Conclusion

- Coside® is a nice “bridge” for students coming from µC and FPGA design to the concepts of an ASIC world, it effectively extents the design flow to system level
- It is quite easy to use, as the hurdle to start with it is quite low (with initial Windows & C/C++ & Simulink experience), libraries help as a starting point
- It is a powerful platform to introduce many different modelling concepts, thanks to the versatility of SystemC and SystemC AMS - IEEE1666(.1)
- Several use cases from the actual lectures were presented, these are by far not the limits of the setup (not shown: Verification, HW/SW codesign, HLS, etc.)

Thank you for your attention!

- Any questions?