A virtual prototyping methodology for timing-accurate simulation of AMS circuits

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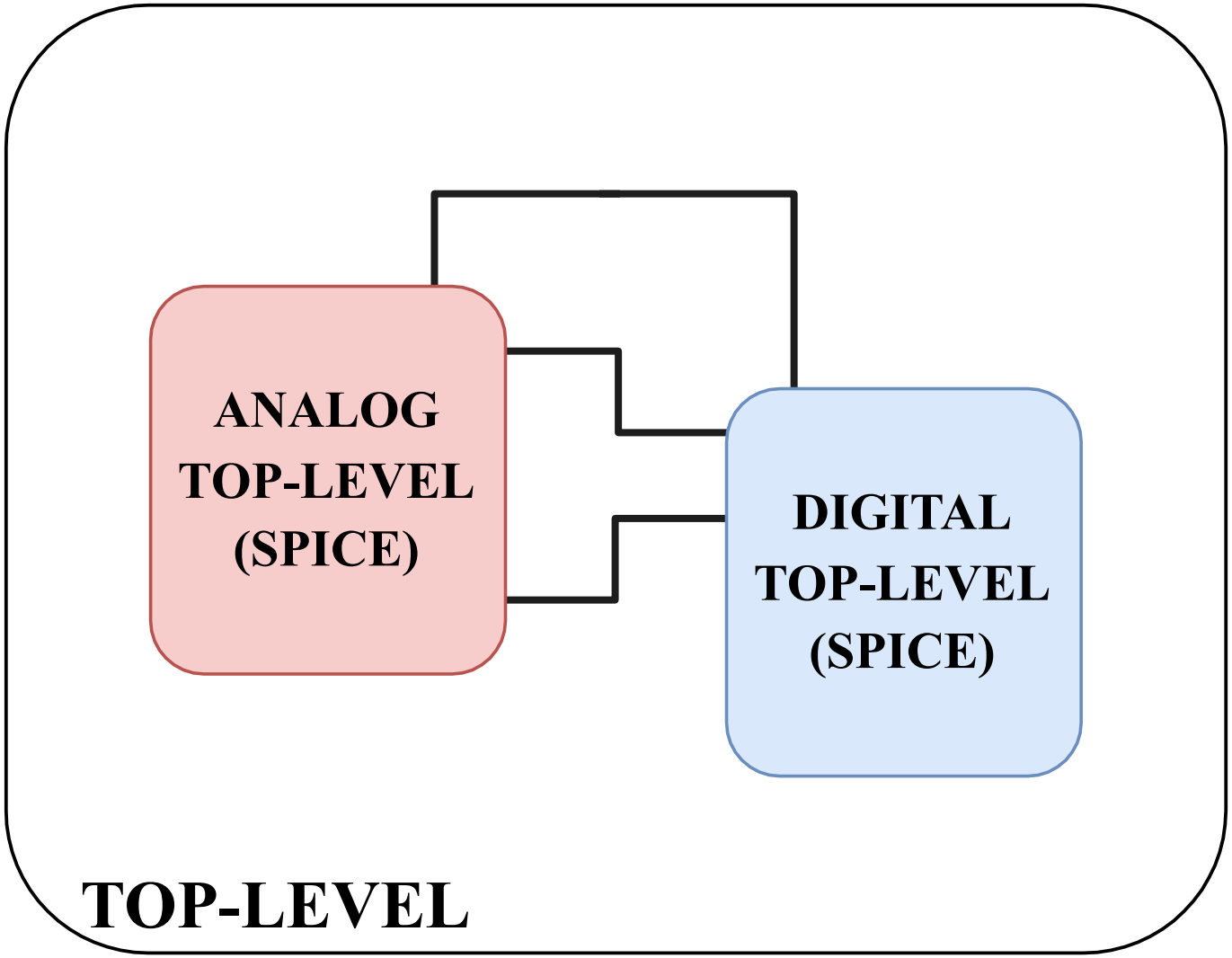
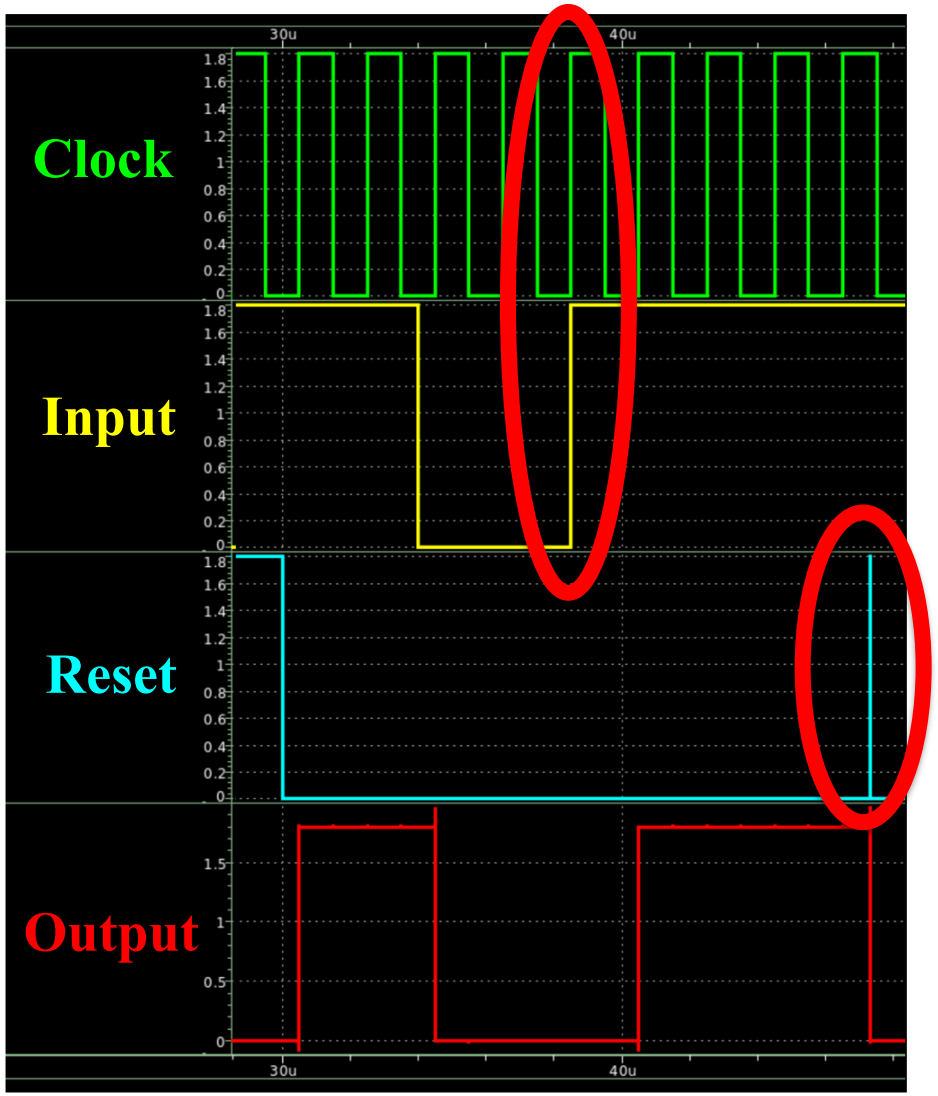
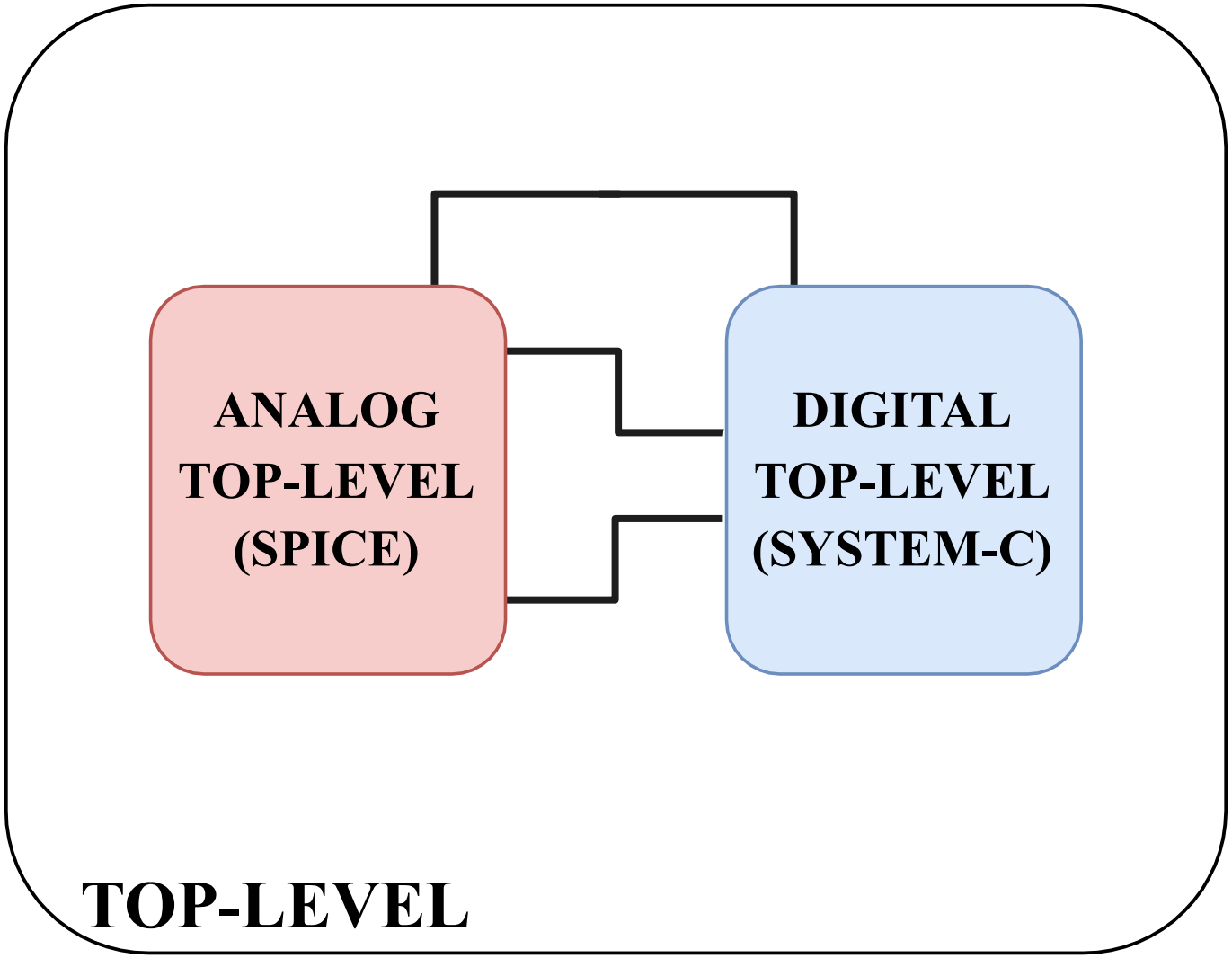
Introduction: Mixed-Signal Flow





Solution: Abstraction of Digital Circuits



- Adds timing checks to digital elements (i.e., flip-flops)
- Maintains digital circuits' timing accuracy (Liberty Data)
- Maintains analog circuits' overall accuracy (kept in SPICE)
- Increases simulation speed (Discrete Events-based digital simulator)
- Improves reusability (library of sub-circuits)

Requirements: Inputs

Liberty Database

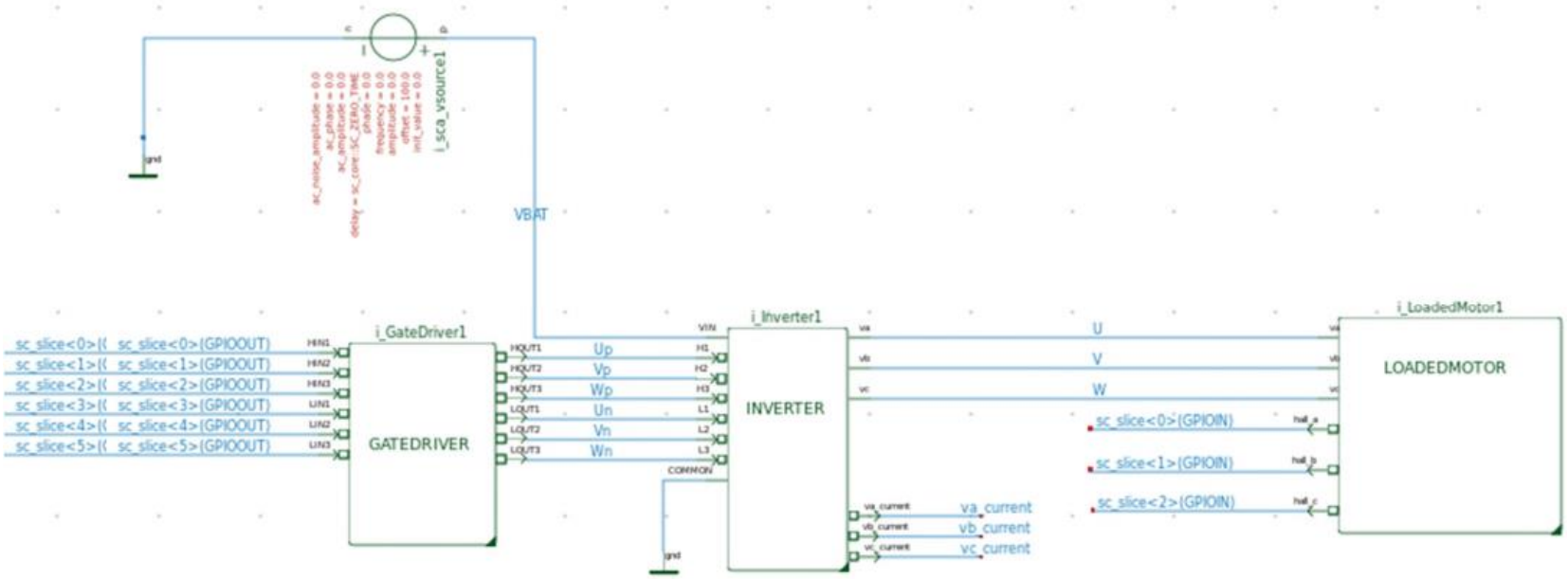
```
cell ("sky130_fd_sc_hs__and2_1") {
  area : 7.992;
  ...
  pin ("A") {
    direction : "input";
    capacitance : 0.0024;
    internal_power () {...} ...
  }
  pin ("X") {
    direction : "output";
    function : "(A&B)";
    ...
    timing () {
      cell_fall ("delay_template13x20") {
      index_1("0.01, 0.01735, ...");
      index_2("0.00, 0.00841, ...");
      values("0.05541, 0.0872, ...",
                "0.05756, 0.08938, ...", ...
  } ... } ... } ... }
```

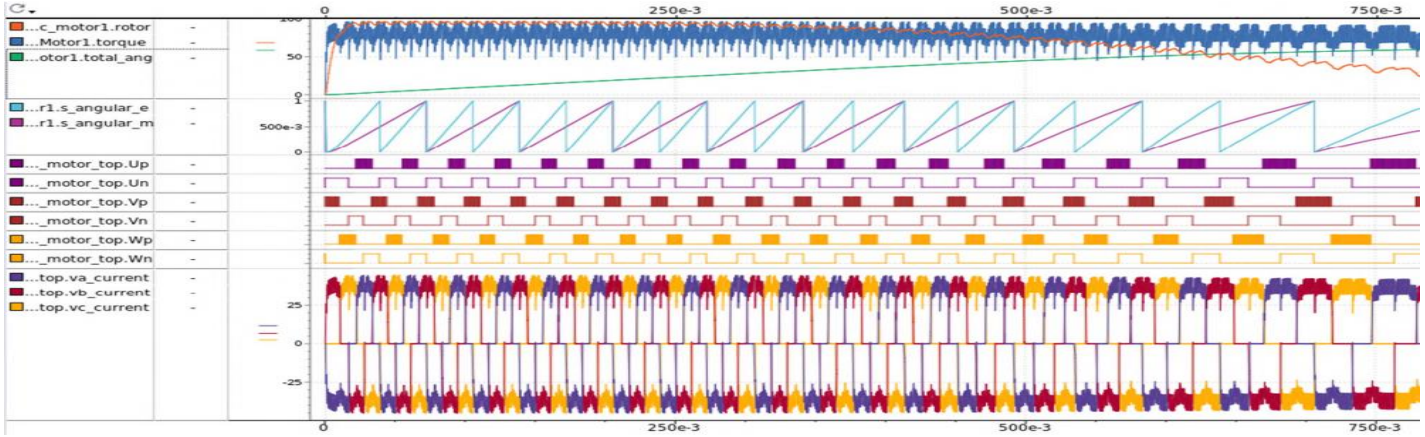
SPICE-level Netlist

```
.include "sky130_fd_pr__nfet_01v8_lvt__tt.spice"
...
.SUBCKT sky130_fd_sc_hs__and2 A B X VGND VNB VPB VPWR
  MMP0 y A VPWR VPB pfet_01v8 m=1 w=0.84 l=0.15 ...
  MMP1 y B VPWR VPB pfet_01v8 m=1 w=0.84 l=0.15 ...
  MMN0 y A sndA VNB nfet_01v8_lvt m=1 w=0.64 l=0.15 ...
  MMN1 sndA B VGND VNB nfet_01v8_lvt m=1 w=0.64 l=0.15 ...
  MMIP0 X y VPWR VPB pfet_01v8 m=1 w=1.12 l=0.15 ...
  MMIN0 X y VGND VNB nfet_01v8_lvt m=1 w=0.74 l=0.15 ...
.ENDS sky130_fd_sc_hs__and2_1
...
.SUBCKT TopLevel6288 A0 A1 ... P31 VGND VNB VPB VPWR
  X0 A3 B0 net1 VGND VNB VPB VPWR sky130_fd_sc_hs_nand2
  ...
  X6 A1 B4 net27 VGND VNB VPB VPWR sky130_fd_sc_hs_and2
  ...
  X84 B12 A0 P6 VGND VNB VPB VPWR sky130_fd_sc_hs_xnor2
.ENDS TopLevel6288
```

SystemC-AMS & COSIDE Environment

- Design, compile, simulate and verify SystemC(AMS) code
- Drag and drop blocks in a schematic
- Create behavioral models for mixed-signal circuits
- Integration with SPICE, other HDLs...
- HW/SW co-simulation, ability to model electrical and mechanical parameters...





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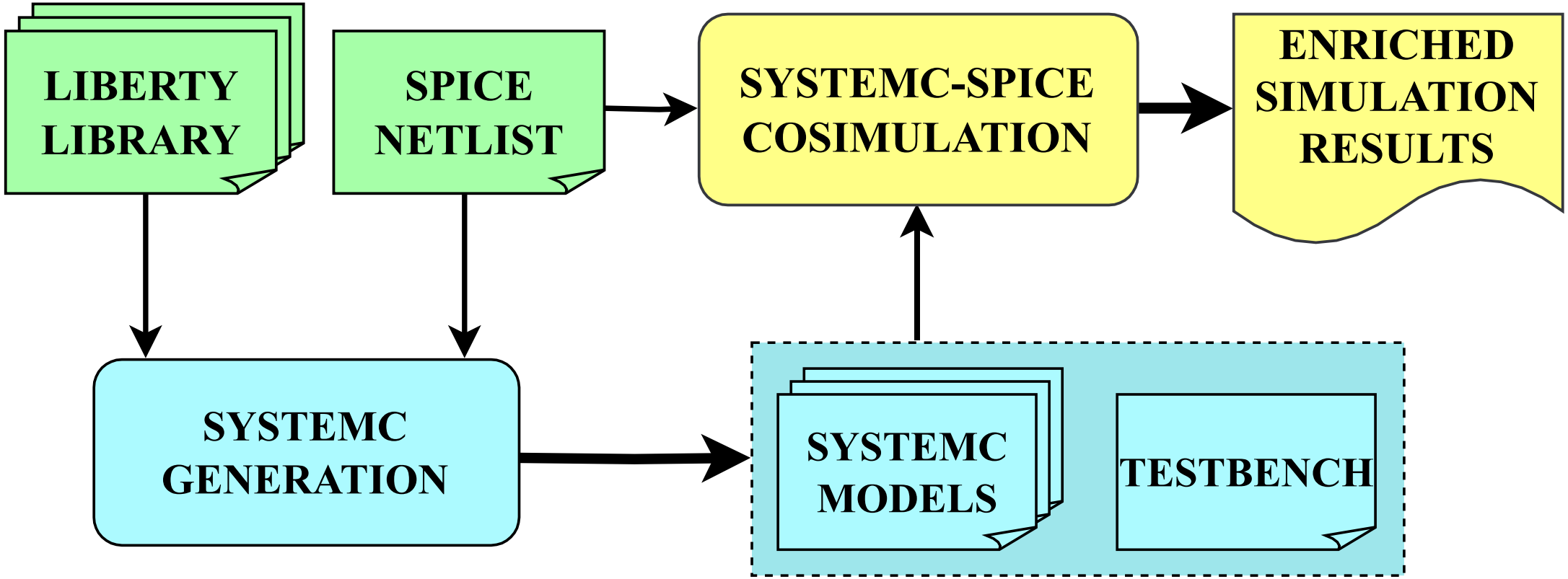
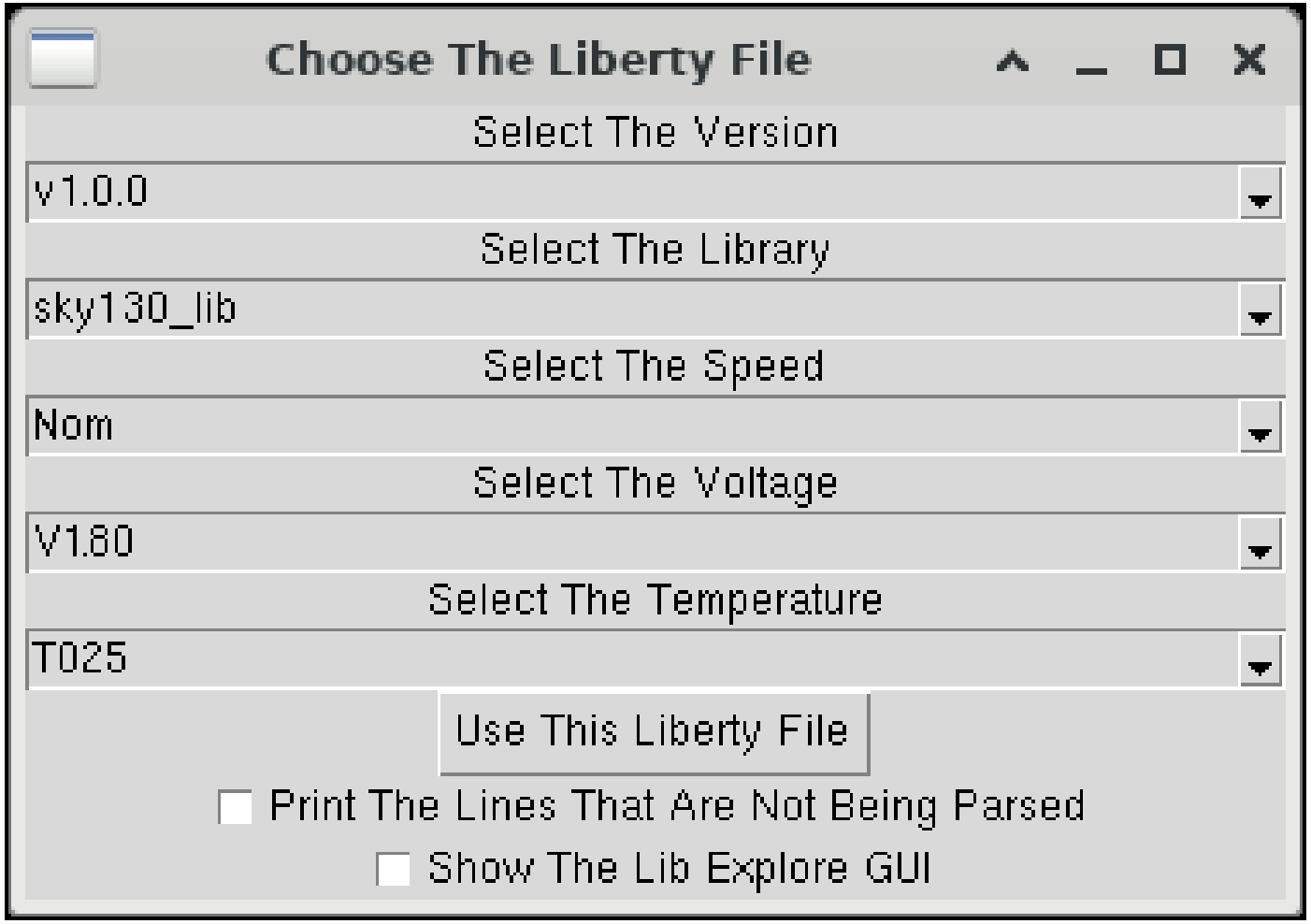
Proposed methodology (0): Top-level View



Proposed methodology (1): Select PVT Corner

- Cell libraries are typically described with multiple corners
- Characterization at different Voltages, Temperatures and with different Process quality
- Many corners to predict the behavior of the system in both nominal conditions and in the most extreme ones
- The library of SystemC standard cells will use a single, selectable corner



Proposed methodology (2): Parse Liberty

Lib Explore

Cells, Pins & Parameters	Path To Reach This Element
sky130_fd_sc_hs__a41oi_1	cell_list[67].name
sky130_fd_sc_hs__a41oi_2	cell_list[68].name
sky130_fd_sc_hs__a41oi_4	cell_list[69].name
sky130_fd_sc_hs__and2_1	cell_list[70].name
Area=7.9920000000	cell_list[70].area
Avg_Leak_Power=0.1384900000	cell_list[70].pleak_avg
Leak_Power_List	cell_list[70].pleak_values
Pin_List	cell_list[70].pin_list
A	cell_list[70].pin_list[0].name
B	cell_list[70].pin_list[1].name
X	cell_list[70].pin_list[2].name
OUTPUT	cell_list[70].pin_list[2].direction
Cap=0.0023000000	cell_list[70].pin_list[2].cap
Min_Cap=	cell_list[70].pin_list[2].min_cap
Max_Cap=0.1485900000	cell_list[70].pin_list[2].max_cap
Function:(A&B)	cell_list[70].pin_list[2].function
Timing_Features_List	cell_list[70].pin_list[2].timing_list
A	cell_list[70].pin_list[2].timing_list[0].name
Timing_Sense:positive_unate	cell_list[70].pin_list[2].timing_list[0].timing_sense
Cell_Fall	cell_list[70].pin_list[2].timing_list[0].idx2_list[0]
Fall_Transition	cell_list[70].pin_list[2].timing_list[0].idx2_list[1]
Cell_Rise	cell_list[70].pin_list[2].timing_list[0].idx2_list[2]
Rise_Transition	cell_list[70].pin_list[2].timing_list[0].idx2_list[3]
Output_Current_Fall	cell_list[70].pin_list[2].timing_list[0].I_fall_list
Output_Current_Rise	cell_list[70].pin_list[2].timing_list[0].I_rise_list
B	cell_list[70].pin_list[2].timing_list[1].name
Internal_Power_List	cell_list[70].pin_list[2].internal_power
sky130_fd_sc_hs__and2_2	cell_list[71].name

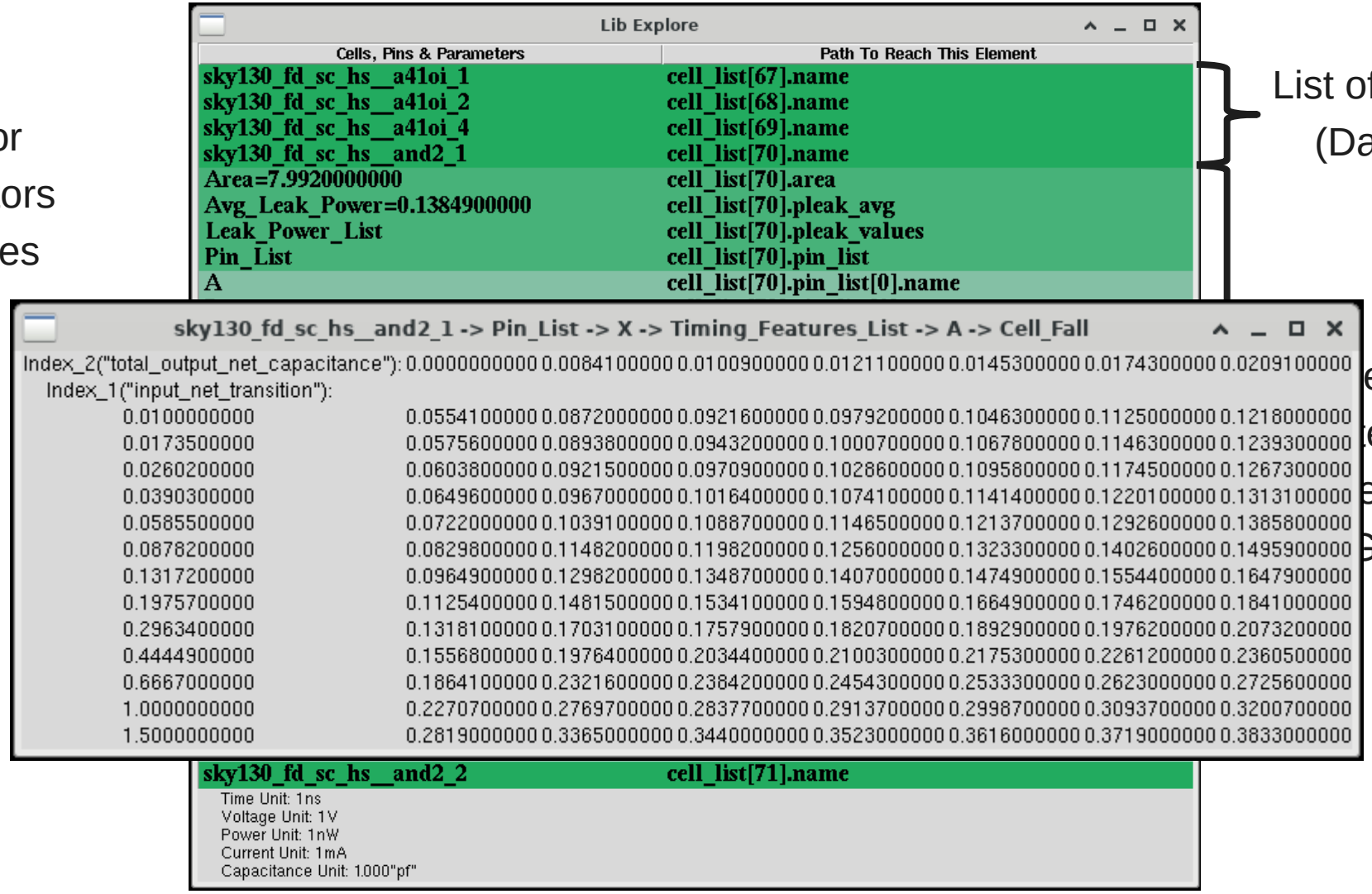
Time Unit: 1ns
Voltage Unit: 1V
Power Unit: 1nW
Current Unit: 1mA
Capacitance Unit: 1.000"pf"

List of library cells (Dark Green)

Hierarchical content of a cell (Green -> Blue Gradient)

Proposed methodology (2): Parse Liberty

Popup GUI for data in 1D vectors and 2D matrixes



List of library cells (Dark Green)

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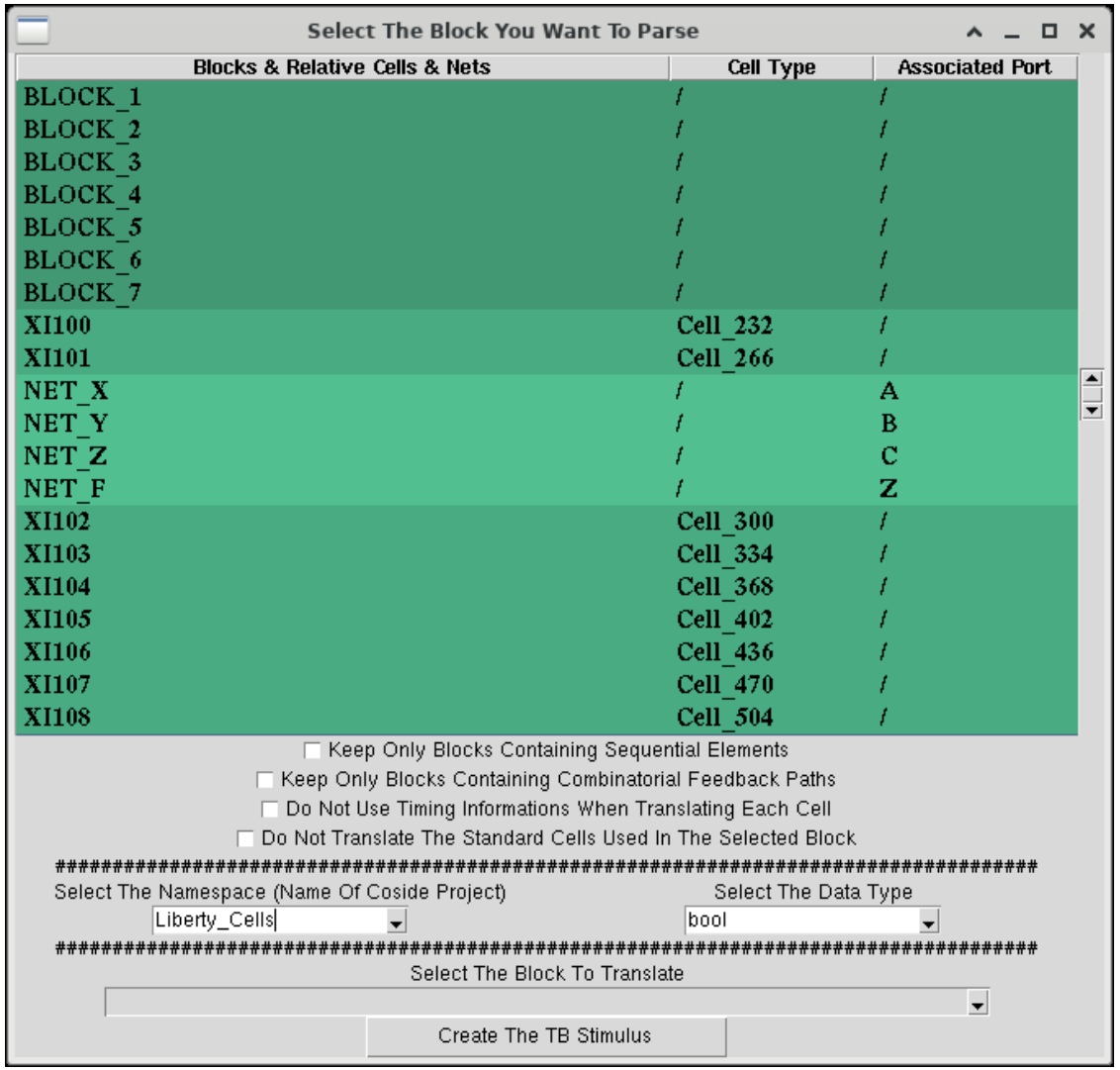
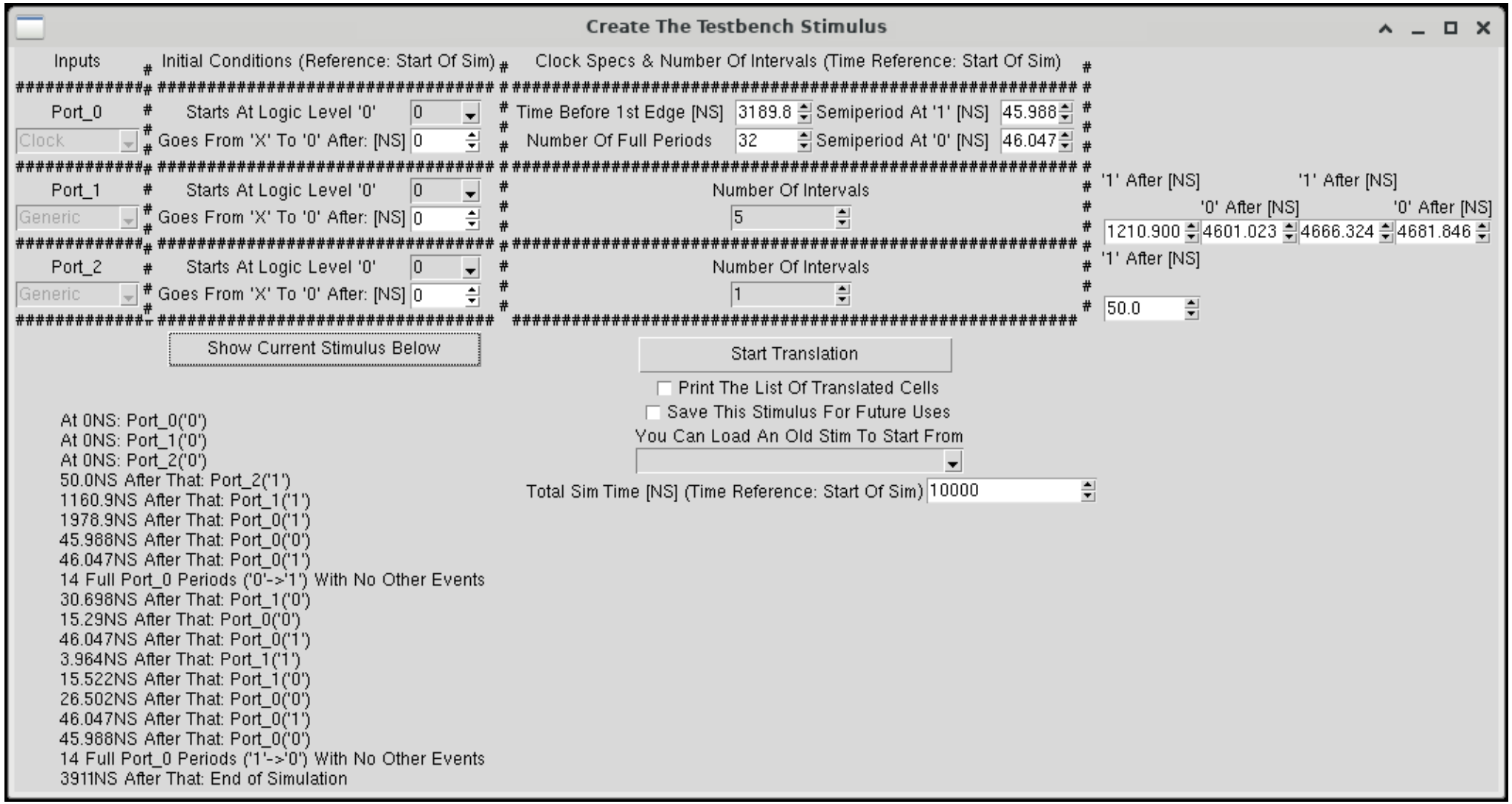
Gradient)

Proposed methodology (3): Parse Netlist

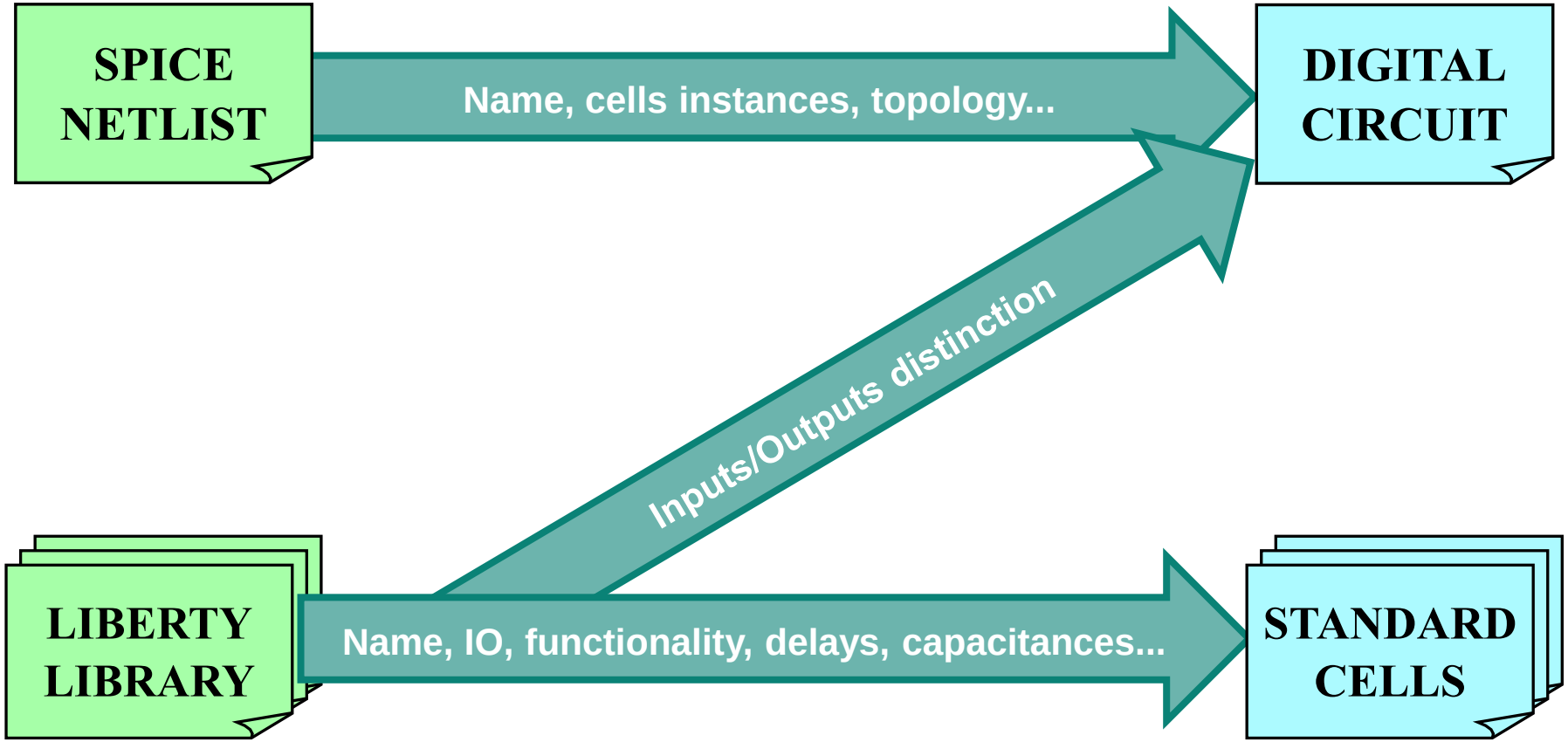
- The script searches for blocks made of standard cells, filtering out the rest
- From each block we sample data about its cells' connections (wires, types of cells, names...)
- Synergy with Liberty data to distinguish INs from OUTs at both cell-level and block-level
- One block is selected and translated to SystemC using the same topology as the netlist



Proposed methodology (4): Testbench Generator



Proposed methodology (5): Module Generation



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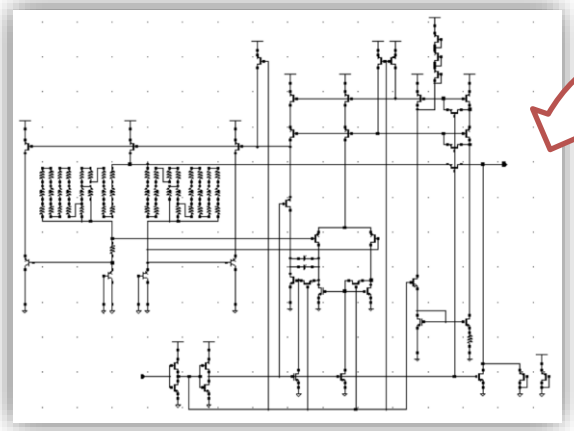
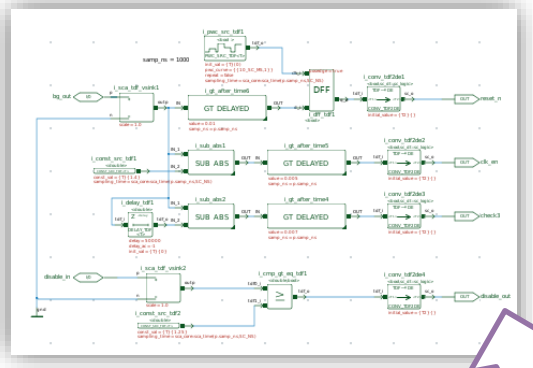
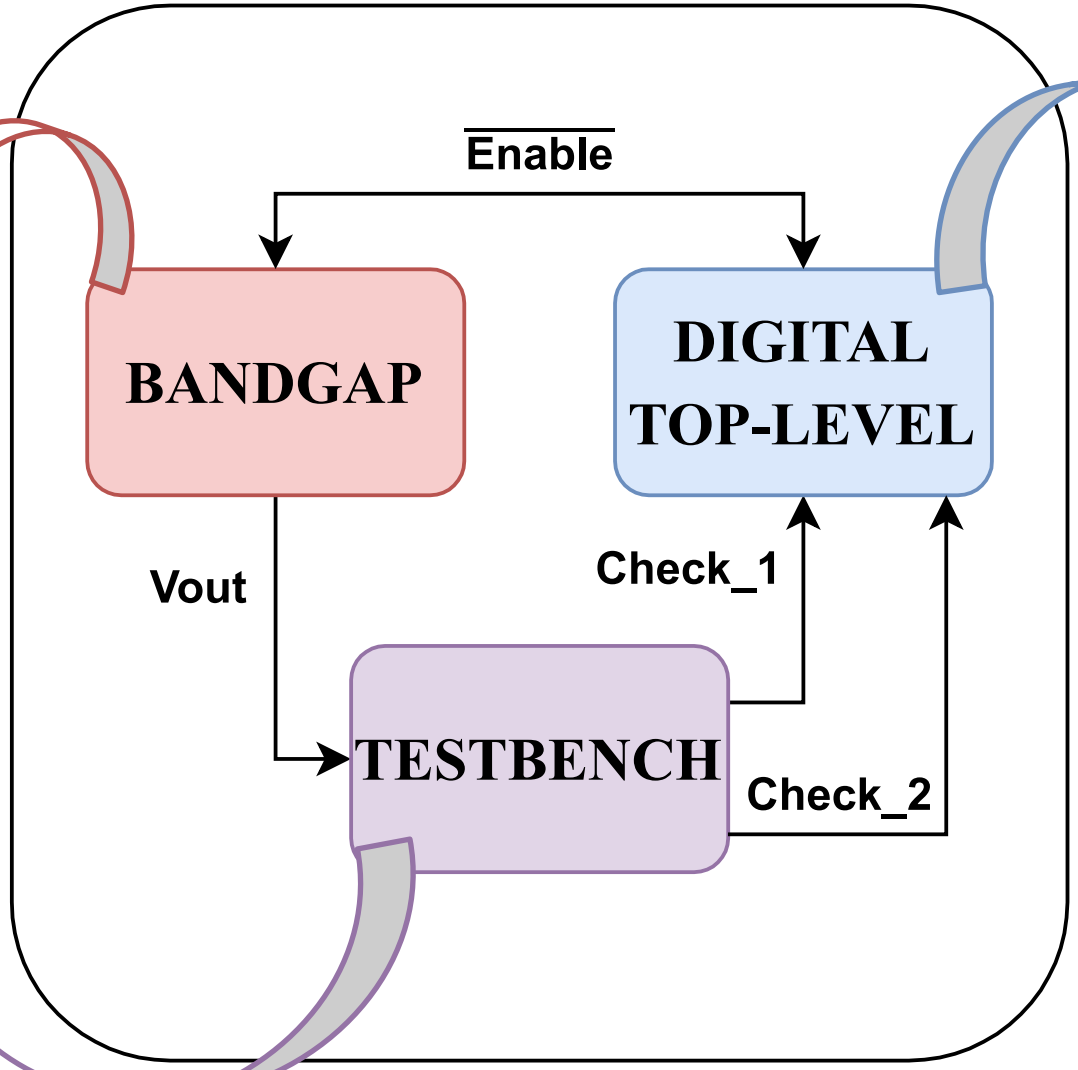
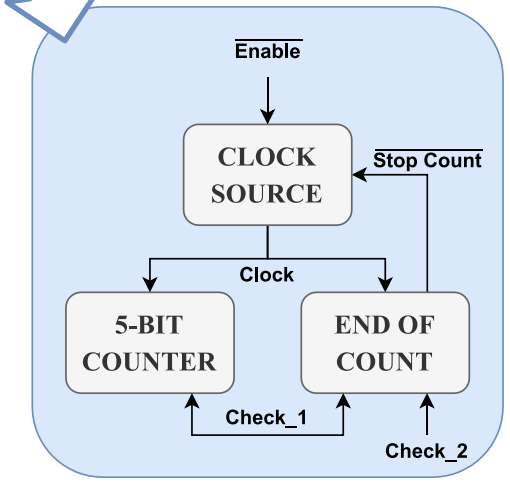
Main Benchmark: Infineon Open-Source Bandgap

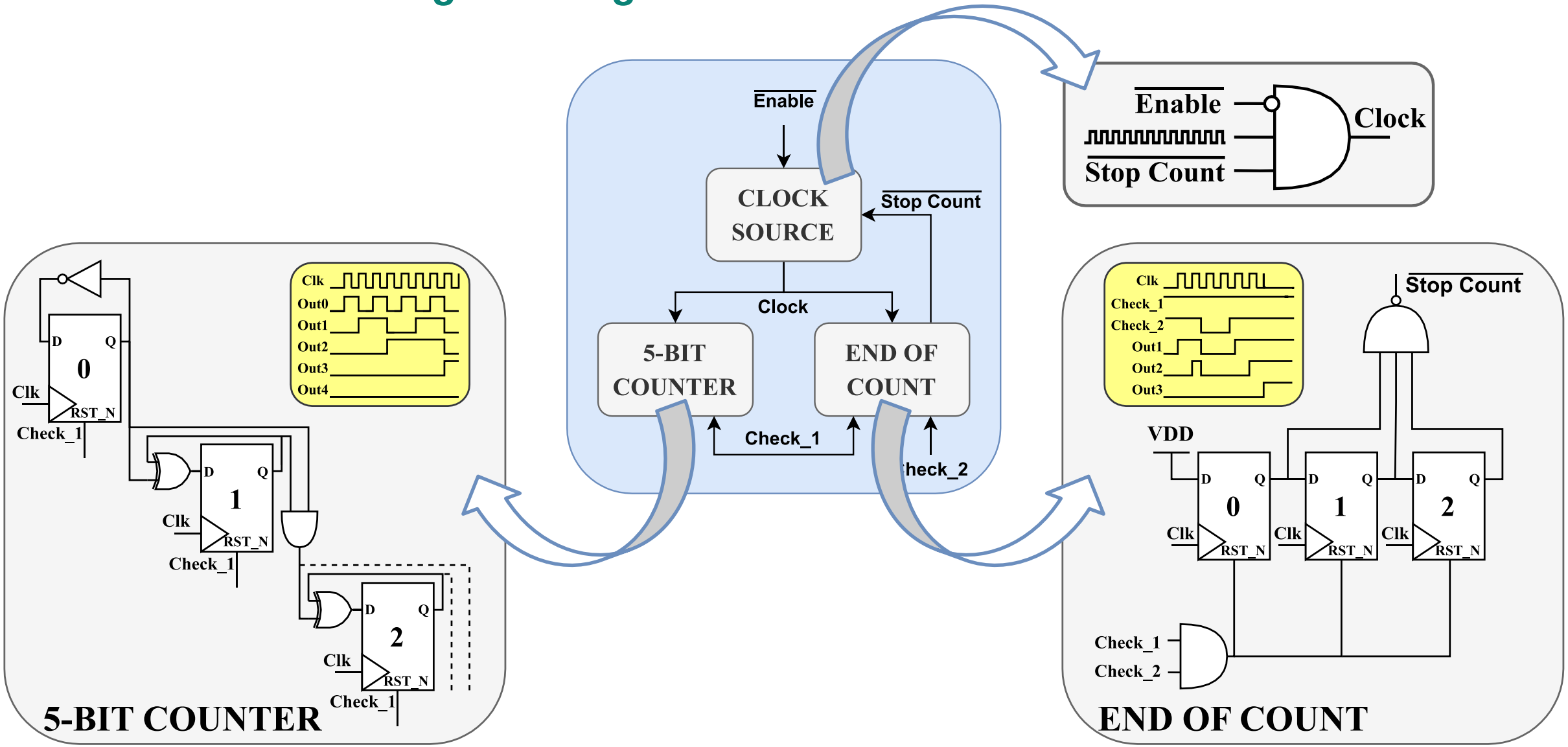




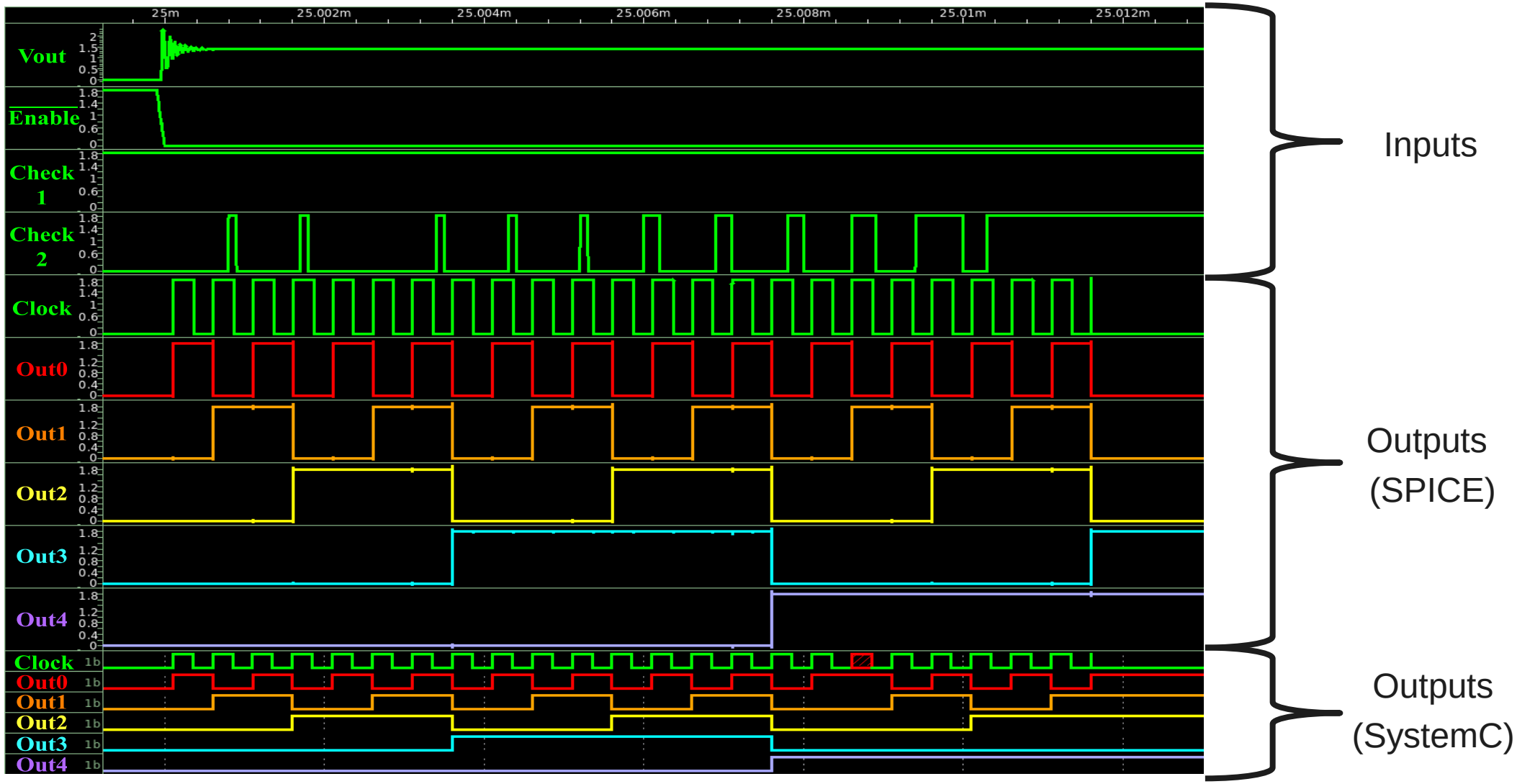




Main Benchmark: Integrated Digital Circuit

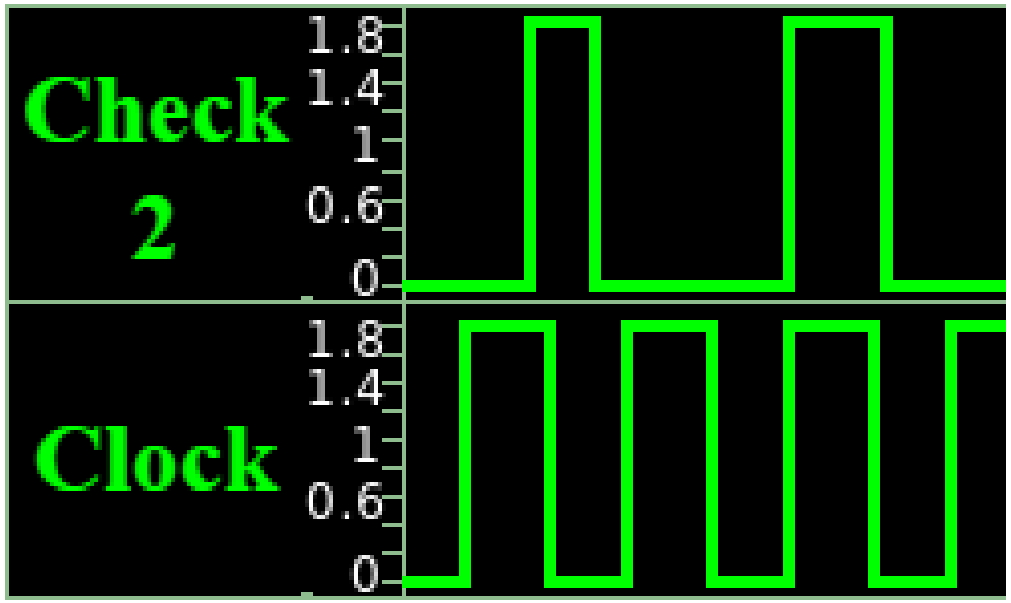


Main Benchmark: Results

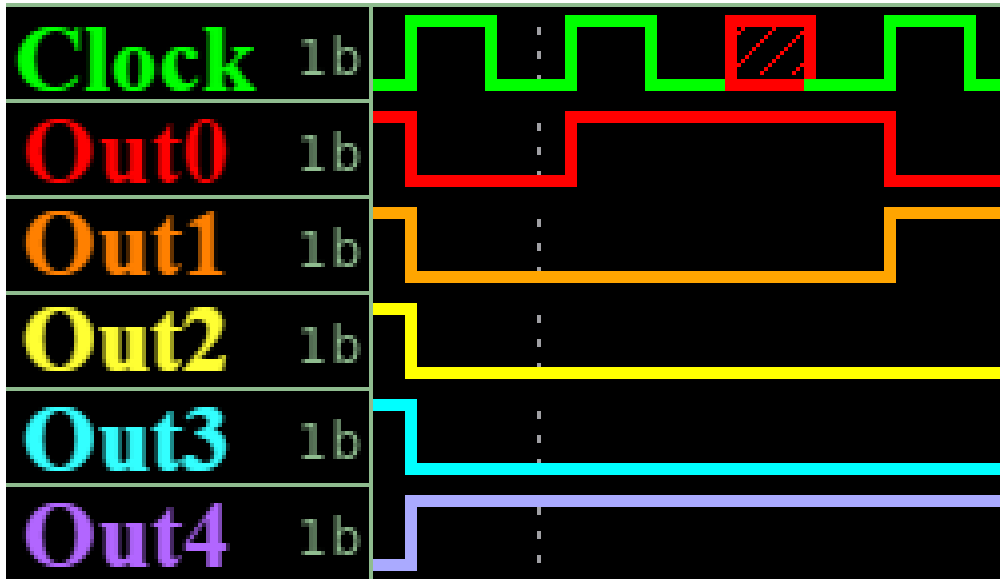


Main Benchmark: Results (Zoom)

Cause



Effects



infineon