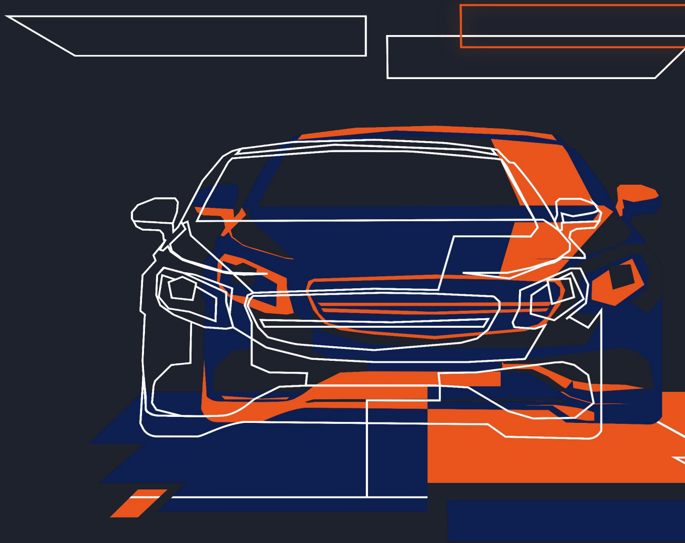
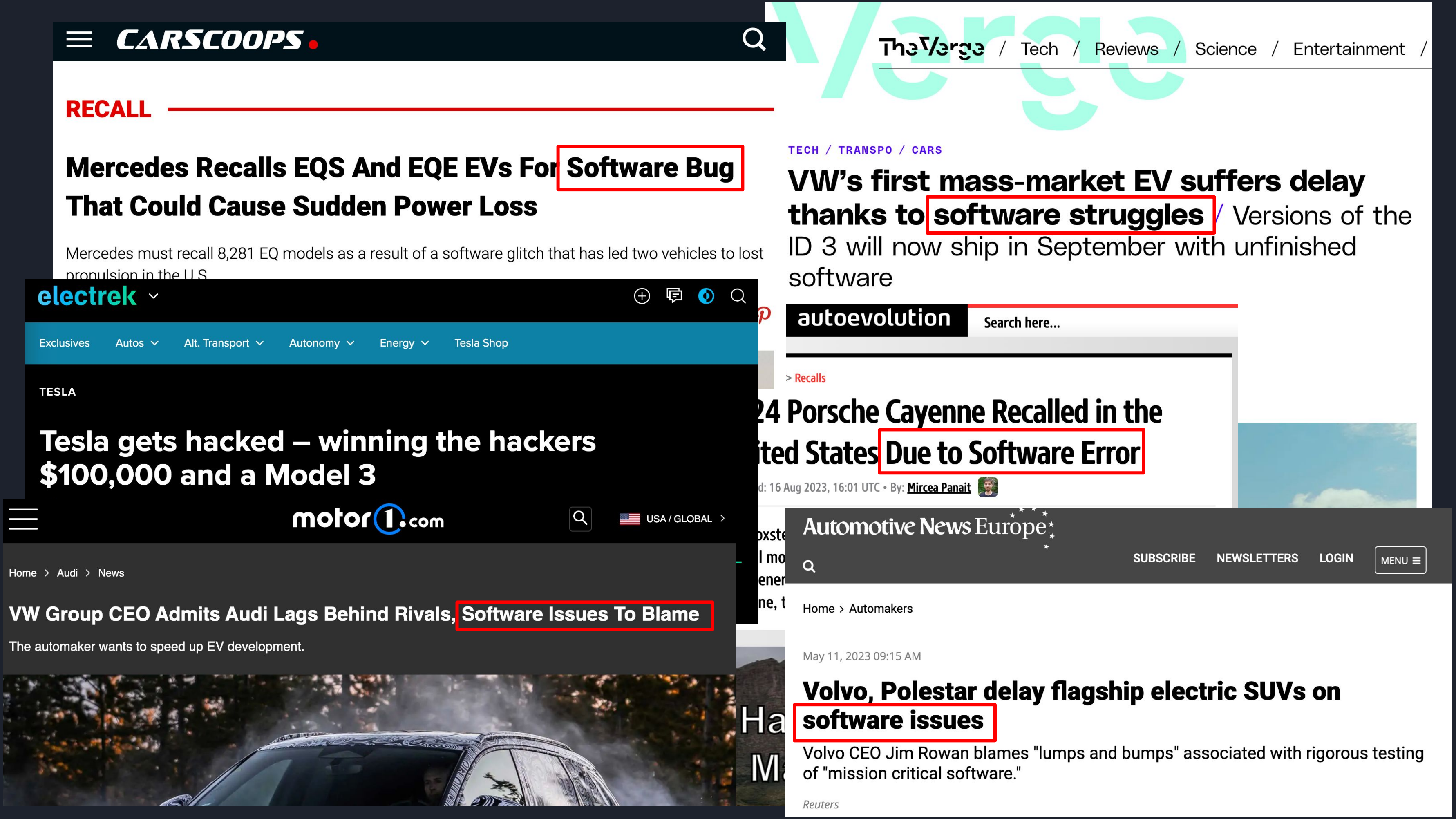
Fast Virtual Platforms for Scalable Software Verification

Lukas Jünger, MachineWare GmbH

lukas@mwa.re



MACHINEWARE



CARSCOOPS

RECALL

Mercedes Recalls EQS And EQE EVs For Software Bug That Could Cause Sudden Power Loss

Mercedes must recall 8,281 EQ models as a result of a software glitch that has led two vehicles to lost propulsion in the U.S.

The Verge / Tech / Reviews / Science / Entertainment /

TECH / TRANSPO / CARS

VW's first mass-market EV suffers delay thanks to software struggles

/ Versions of the ID 3 will now ship in September with unfinished software

electrek

Exclusives · Autos · Alt. Transport · Autonomy · Energy · Tesla Shop

TESLA

Tesla gets hacked – winning the hackers $100,000 and a Model 3

autoevolution

Search here...

> Recalls

24 Porsche Cayenne Recalled in the ited States Due to Software Error

d: 16 Aug 2023, 16:01 UTC • By: Mircea Panait

oxste
l mo
ener
ne, t

motor1.com

USA / GLOBAL

Home > Audi > News

VW Group CEO Admits Audi Lags Behind Rivals, Software Issues To Blame

The automaker wants to speed up EV development.

Ha
Ma

Automotive News Europe

SUBSCRIBE · NEWSLETTERS · LOGIN · MENU

Home > Automakers

May 11, 2023 09:15 AM

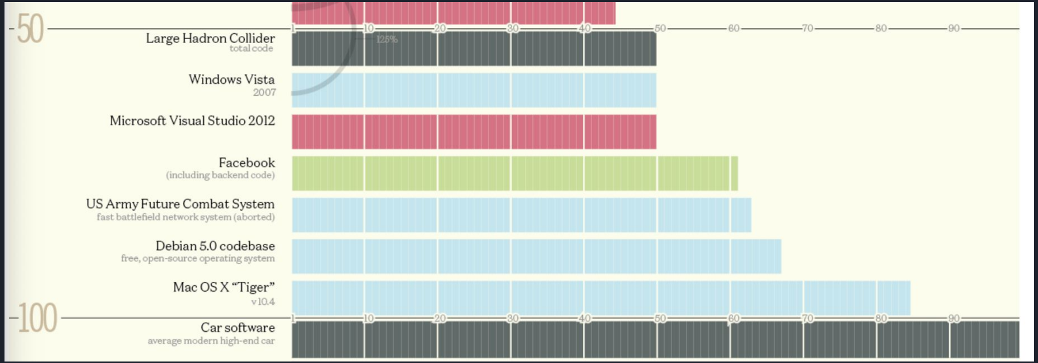
Volvo, Polestar delay flagship electric SUVs on software issues

Volvo CEO Jim Rowan blames "lumps and bumps" associated with rigorous testing of "mission critical software."

Reuters

Motivation

- Software challenges
  - Complexity is rising
    - Car: >100 Mio. lines of code
  - Security & safety critical
  - Quality is key

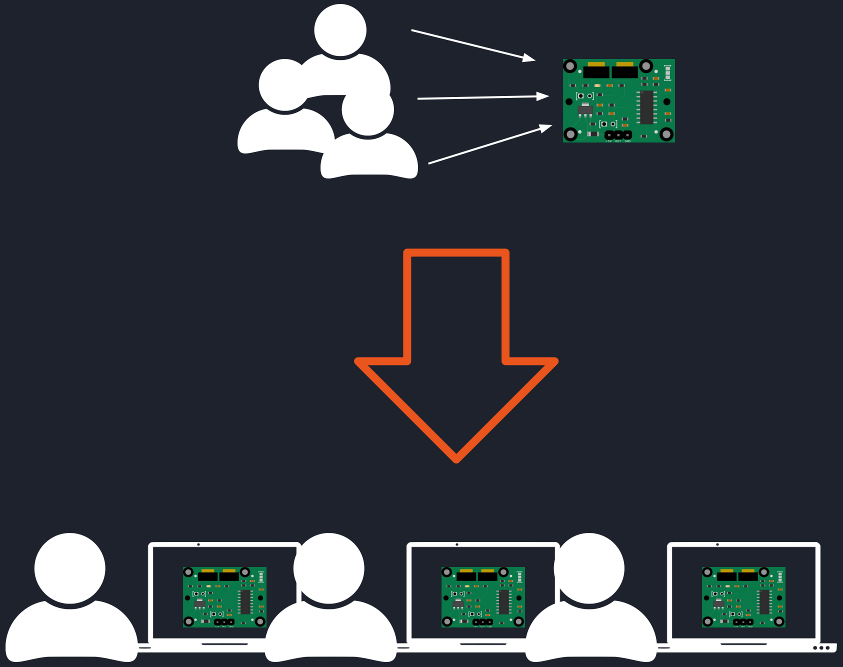


https://informationisbeautiful.net/visualizations/million-lines-of-code/

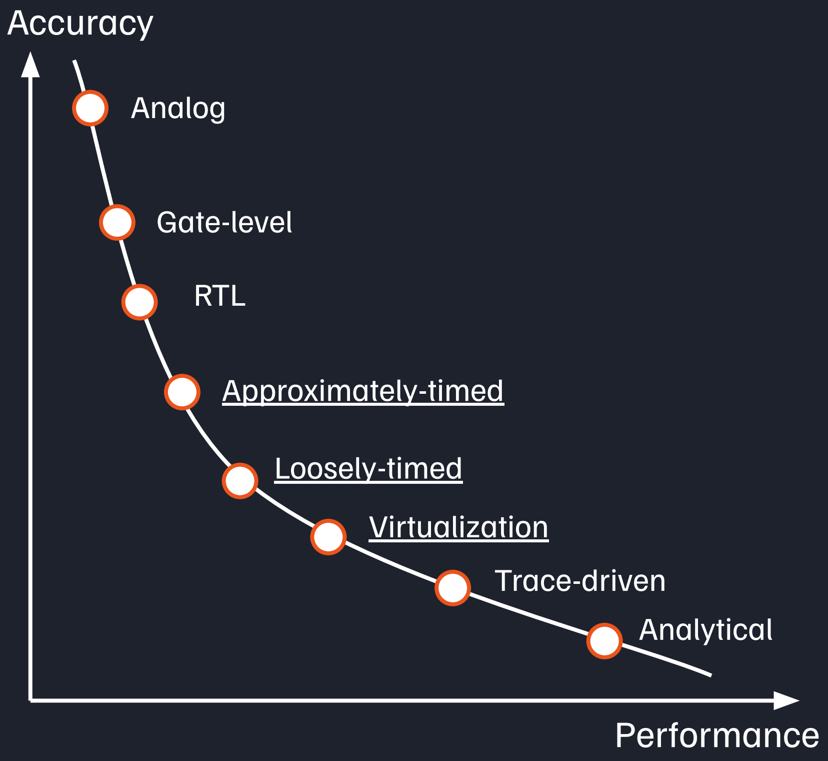
- Bad software is dangerous and expensive
  - Accidents, recalls, liability for hacks, maintenance
- Problem: Testing is
  - Hard to automate, hard to scale, limited by hardware resources

Virtual Prototyping

- Virtual Platform: Full System Simulation
- Indispensable in software development
    - Everising SW and HW complexity
- Advantages over physical prototypes
    - Available earlier (shift-left methodology)
    - Full flexibility, deep introspection
    - Non-intrusive debug
    - Scalability



Simulation Abstraction Levels and Use Cases

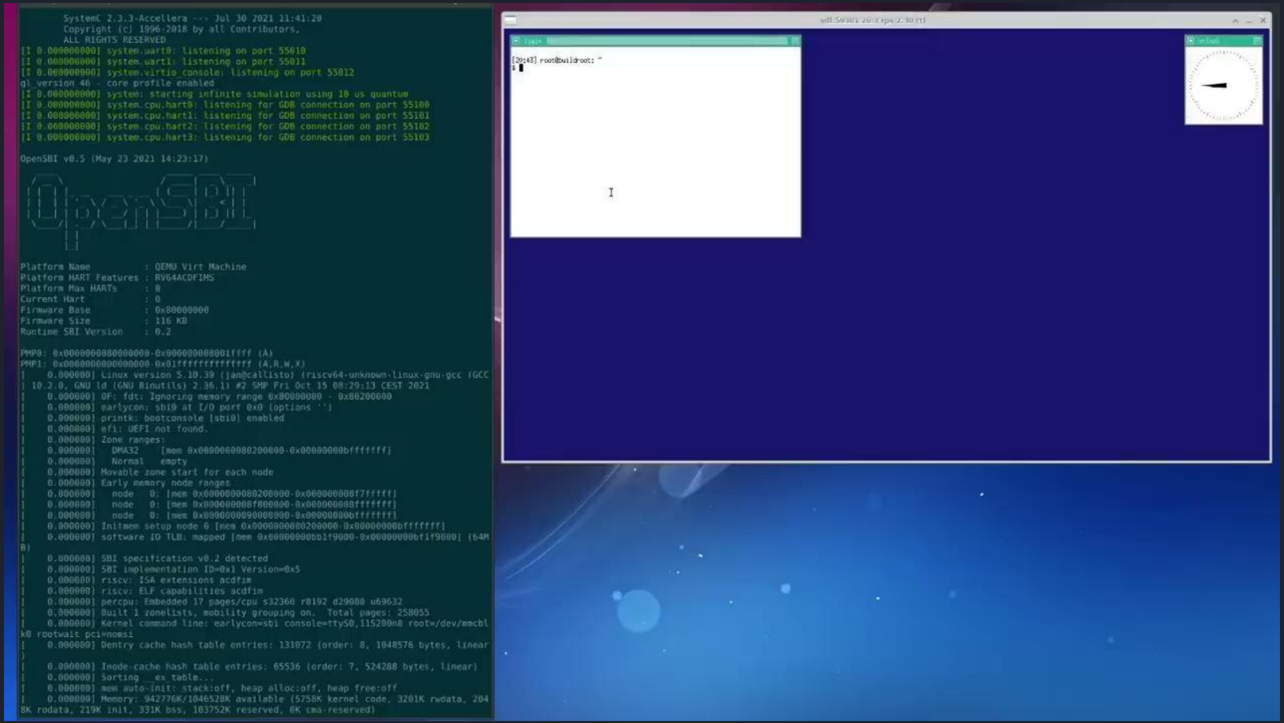


- Many different techniques available
- No silver bullets
  - Right tool for the right job

Transaction Level Modeling (TLM):

- Approximately-timed
  - Architecture exploration, interconnect
- Loosely-timed
  - Early SW development & verification
- Virtualization
  - Regression, SW development

Demo



```
        SystemC 2.3.3-Accellera --- Jul 30 2021 11:41:20
        Copyright (c) 1996-2018 by all Contributors,
        ALL RIGHTS RESERVED
[I 0.000000000] system.uart0: listening on port 55010
[I 0.000000000] system.uart1: listening on port 55011
[I 0.000000000] system.virtio_console: listening on port 55012
gl_version 46 - core profile enabled
[I 0.000000000] system: starting infinite simulation using 10 us quantum
[I 0.000000000] system.cpu.hart0: listening for GDB connection on port 55100
[I 0.000000000] system.cpu.hart1: listening for GDB connection on port 55101
[I 0.000000000] system.cpu.hart2: listening for GDB connection on port 55102
[I 0.000000000] system.cpu.hart3: listening for GDB connection on port 55103

OpenSBI v0.5 (May 23 2021 14:23:17)
   ____                    _____ ____ _____
  / __ \                  / ____|  _ \_   _|
 | |  | |_ __   ___ _ __ | (___ | |_) || |
 | |  | | '_ \ / _ \ '_ \ \___ \|  _ < | |
 | |__| | |_) |  __/ | | |____) | |_) || |_
  \____/| .__/ \___|_| |_|_____/|____/_____|
        | |
        |_|

Platform Name          : QEMU Virt Machine
Platform HART Features : RV64ACDFIMS
Platform Max HARTs     : 8
Current Hart           : 0
Firmware Base          : 0x80000000
Firmware Size          : 116 KB
Runtime SBI Version    : 0.2

PMP0: 0x0000000080000000-0x000000008001ffff (A)
PMP1: 0x0000000000000000-0x01ffffffffffffff (A,R,W,X)
[    0.000000] Linux version 5.10.39 (jan@callisto) (riscv64-unknown-linux-gnu-gcc (GCC
) 10.2.0, GNU ld (GNU Binutils) 2.36.1) #2 SMP Fri Oct 15 08:29:13 CEST 2021
[    0.000000] OF: fdt: Ignoring memory range 0x80000000 - 0x80200000
[    0.000000] earlycon: sbi0 at I/O port 0x0 (options '')
[    0.000000] printk: bootconsole [sbi0] enabled
[    0.000000] efi: UEFI not found.
[    0.000000] Zone ranges:
[    0.000000]   DMA32    [mem 0x0000000080200000-0x00000000bfffffff]
[    0.000000]   Normal   empty
[    0.000000] Movable zone start for each node
[    0.000000] Early memory node ranges
[    0.000000]   node   0: [mem 0x0000000080200000-0x000000008f7fffff]
[    0.000000]   node   0: [mem 0x000000008f800000-0x000000008fffffff]
[    0.000000]   node   0: [mem 0x0000000090000000-0x00000000bfffffff]
[    0.000000] Initmem setup node 0 [mem 0x0000000080200000-0x00000000bfffffff]
[    0.000000] software IO TLB: mapped [mem 0x00000000bb1f9000-0x00000000bf1f9000] (64M
B)
[    0.000000] SBI specification v0.2 detected
[    0.000000] SBI implementation ID=0x1 Version=0x5
[    0.000000] riscv: ISA extensions acdfim
[    0.000000] riscv: ELF capabilities acdfim
[    0.000000] percpu: Embedded 17 pages/cpu s32360 r8192 d29080 u69632
[    0.000000] Built 1 zonelists, mobility grouping on.  Total pages: 258055
[    0.000000] Kernel command line: earlycon=sbi console=ttyS0,115200n8 root=/dev/mmcbl
k0 rootwait pci=nomsi
[    0.000000] Dentry cache hash table entries: 131072 (order: 8, 1048576 bytes, linear
)
[    0.000000] Inode-cache hash table entries: 65536 (order: 7, 524288 bytes, linear)
[    0.000000] Sorting __ex_table...
[    0.000000] mem auto-init: stack:off, heap alloc:off, heap free:off
[    0.000000] Memory: 942776K/1046528K available (5758K kernel code, 3201K rwdata, 204
8K rodata, 219K init, 331K bss, 103752K reserved, 0K cma-reserved)
```

```
[20:43] root@buildroot: ~
$ 
```

How to build a fast Simulator (for SW verification) ?

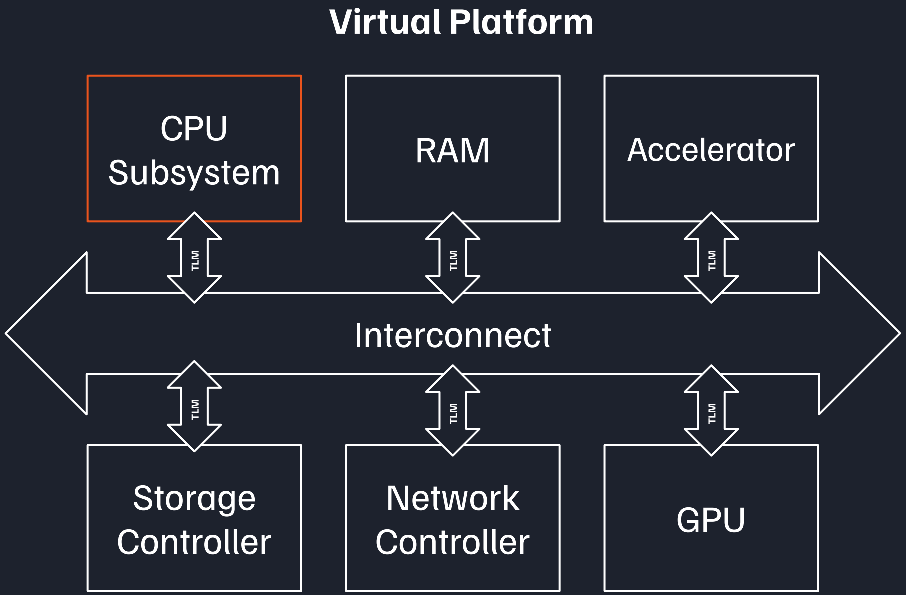
- CPU model executes software
  - Performance dominates VP

Use Case: Early SW development

- Pre-silicon, No HW available
- Fast SW models required

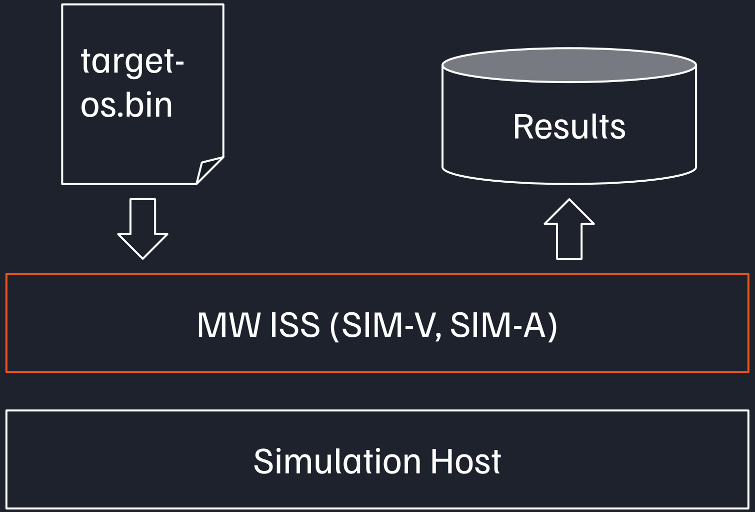
Use Case: Regression Testing

- HW available, but limited scalability
- HW acceleration possible



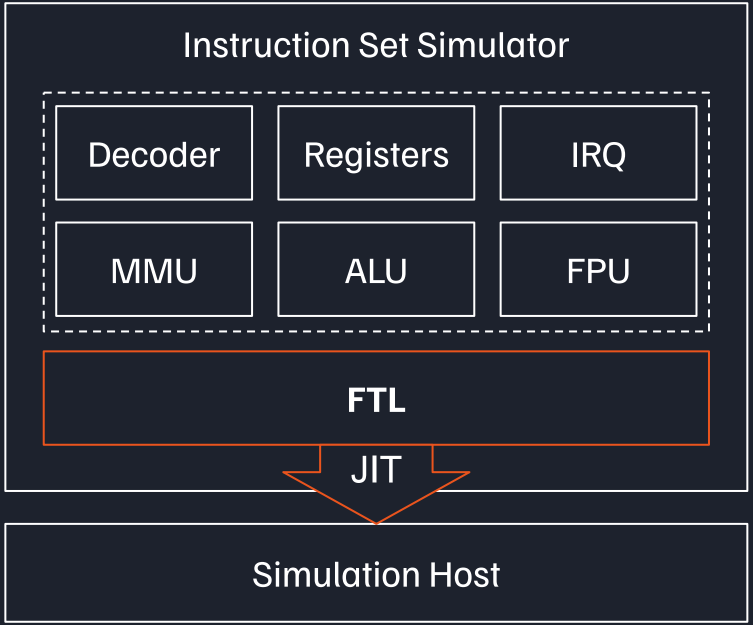
MachineWare Instruction Set Simulators

- Fast, functional simulators
- SW development and verification
- Architecture exploration
- Shift-left: Better software earlier
- Easy to use and integrate
  - Intuitive API and user interface
  - Well documented
  - Bring your own environment



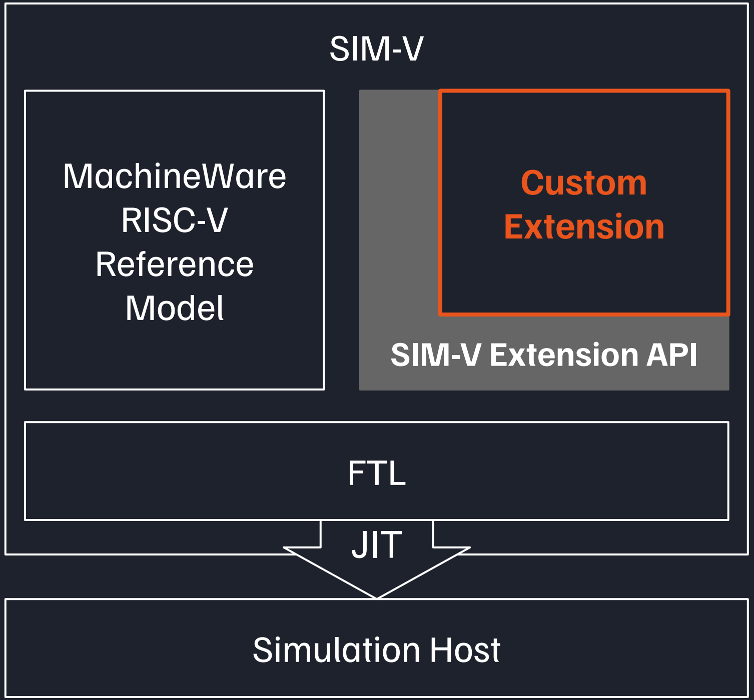
Fast Translator Library

- Processor Modeling Toolkit
- Model your processor in C++
- Partially automated modeling flow
- Fast JIT binary translation
- No target software limitations
- Custom instrumentation
- Custom extensions



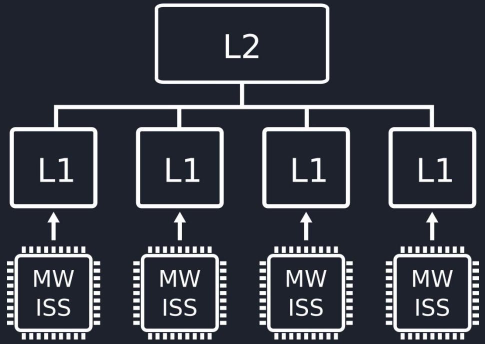
SIM-V Custom Extensions

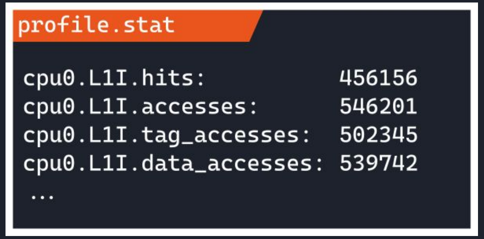
- Customization is a RISC-V USP
  - Add custom instructions, registers, CSRs, …
- SDK for extensions development
  - No modifications to SIM-V
  - Extension automatically loaded
  - Easy to use
- Leverage FTL for performance



FTL Observer Cache Models

- Instrument memory transactions
  - Cache receives addresses and maintenance operations
- Analyze statistics
  - Numerous statistics allow to asses cache and application performance
- Model custom cache hierarchies




profile.stat

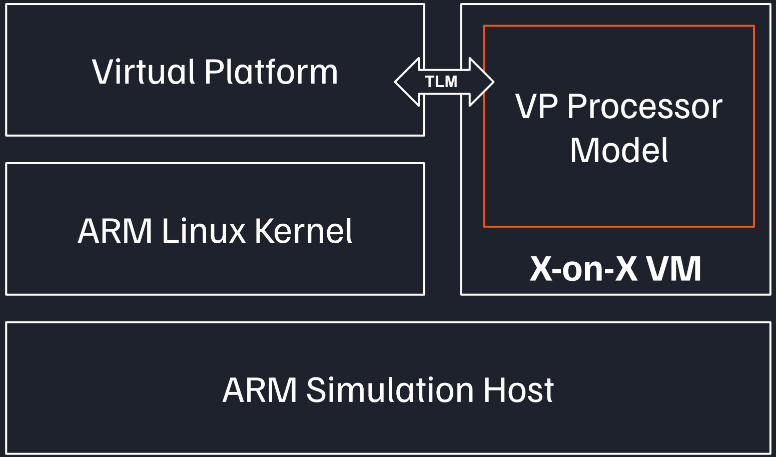
```
cpu0.L1I.hits:          456156
cpu0.L1I.accesses:      546201
cpu0.L1I.tag_accesses:  502345
cpu0.L1I.data_accesses: 539742
 ...
```

ARM-on-ARM

- Traditionally X-on-Y (e.g. ARM on X86)
- Unavoidable ISS overhead ~5-10x
    - No 1-1 instruction mapping
    - In-memory processor state

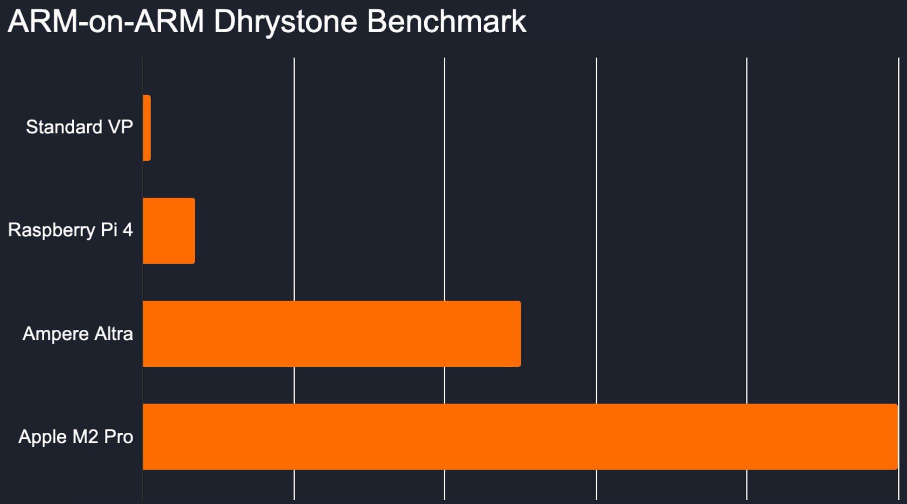
How about X-on-X?

- Encapsulate processor model in VM
- Regular TLM-based VP
- ~80% of native performance

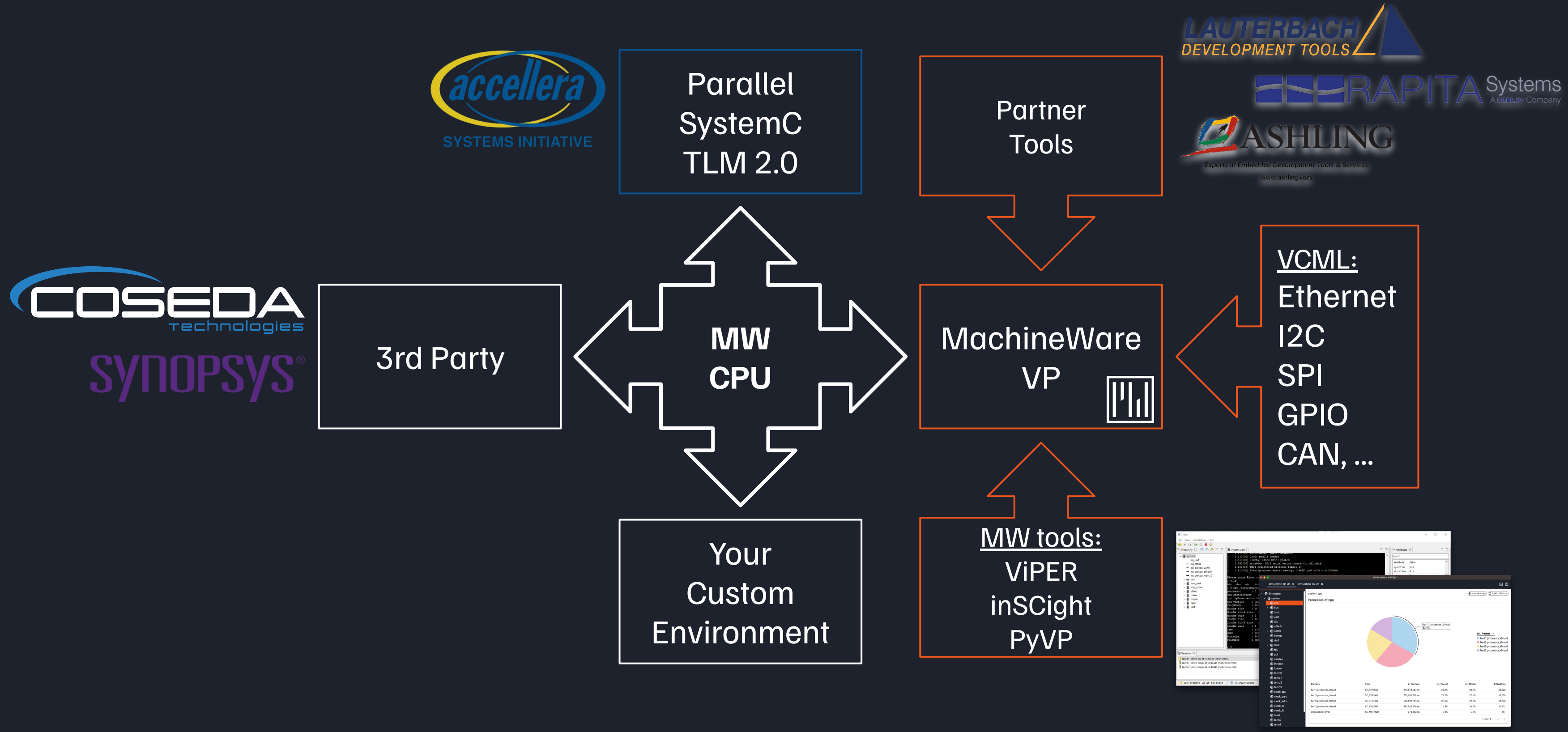


ARM-on-ARM Dhrystone Benchmark

- Dhrystone benchmark measures numeric compute performance
- Upper performance bound
- On good hardware significant boost
- Limited to host HW



Interoperability



accellera SYSTEMS INITIATIVE

Parallel SystemC TLM 2.0

Partner Tools

LAUTERBACH DEVELOPMENT TOOLS

RAPITA Systems

ASHLING Experts in Embedded Development Tools & Services www.ashling.com

COSEDA technologies

SYNOPSYS®

3rd Party

MW CPU

MachineWare VP

VCML:
Ethernet
I2C
SPI
GPIO
CAN, ...

Your Custom Environment

MW tools:
ViPER
inSCight
PyVP

Partners

ANDES TECHNOLOGY

ASHLING

Experts in Embedded Development Tools & Services

www.ashling.com

RAPITA SYSTEMS

A DANLAW COMPANY

LAUTERBACH DEVELOPMENT TOOLS

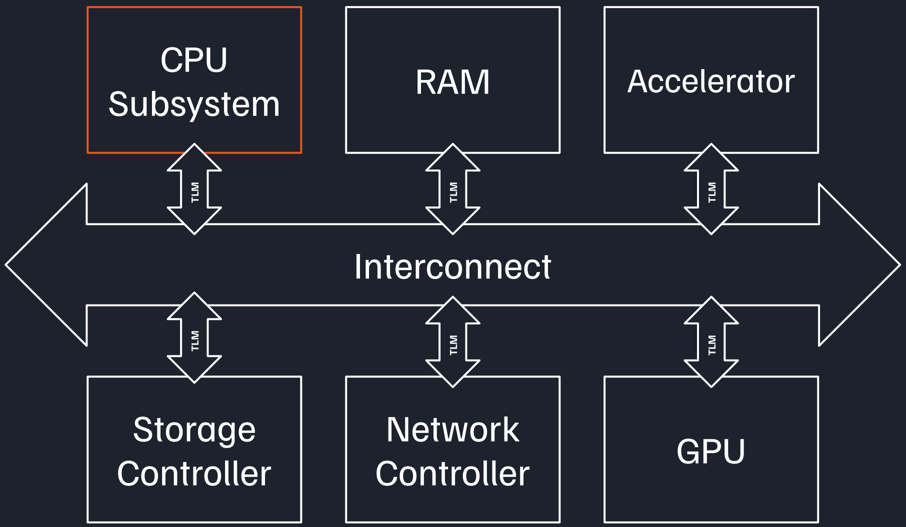
COSEDA technologies

TASKING®

Summary

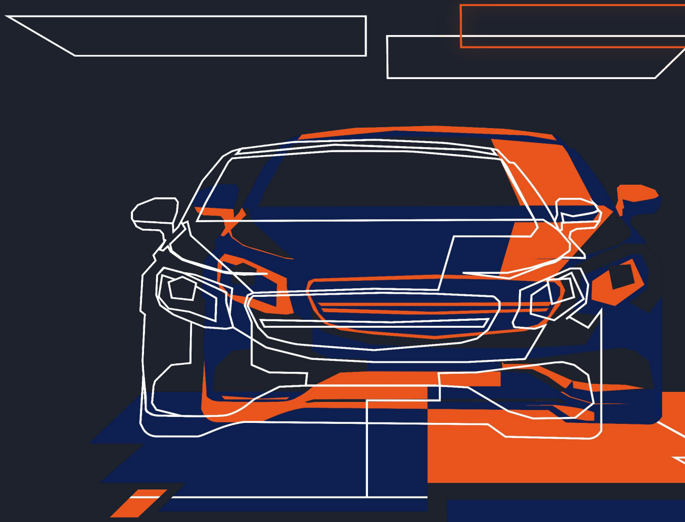
- CPU models are key for SW verification
  - Fast, parallel ISS required
- Model interoperability important
  - Good starting point: SystemC TLM-2.0
- Host HW acceleration promising
  - Utilize host processor, GPU, …
- No silver bullets

Virtual Platform



Thanks!

Questions?



MachineWare