Using virtualGTM with Coside – advantages, opportunities

AE/PAI-IP 06.12.2023 Jürgen Hanisch

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Using virtualGTM with Coside

Agenda

- What is the GTM-IP and where is it used
- What is the virtualGTM
- Who should know/ use the virtualGTM ?
- Opportunities of/ with virtualGTM
- Introduction to use cases and using virtualGTM in Coside

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Using virtualGTM with Coside

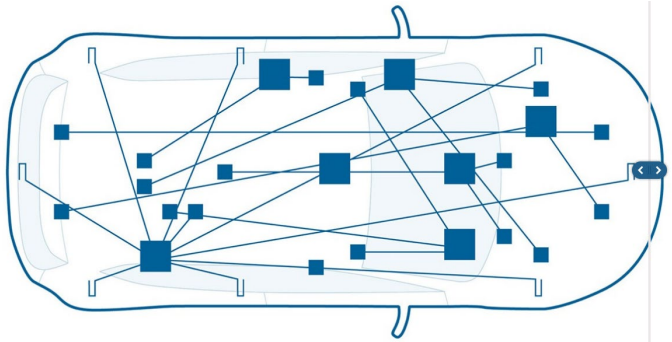
What is the GTM-IP and where is it used

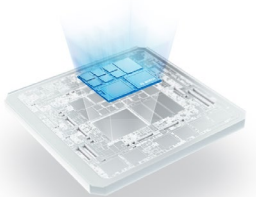
Multiple ECUs are built in cars to fullfill all necessary functions

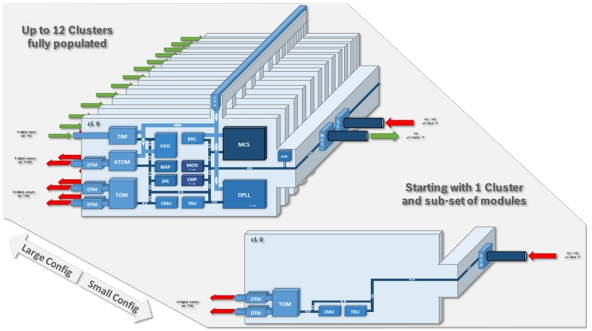
ECUs are typically built up with one/ multiple microcontrollers

An automotive microcontroller can embed one/ multiple GTM-IP units

GTM-IP functionality can scale depending on application usage







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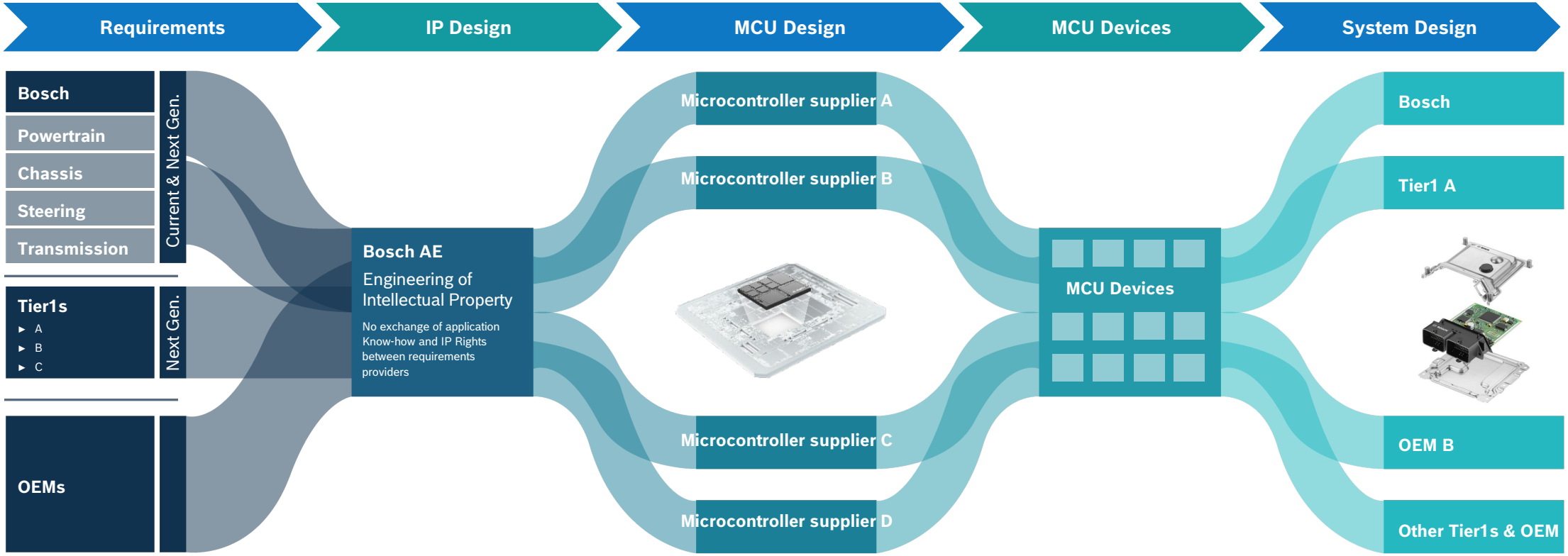
GTM-IP – Legal Framework
From requirements to solutions



Protection by contract and/or NDA

Bosch AE distributes right of the requirements provider to S/C suppliers

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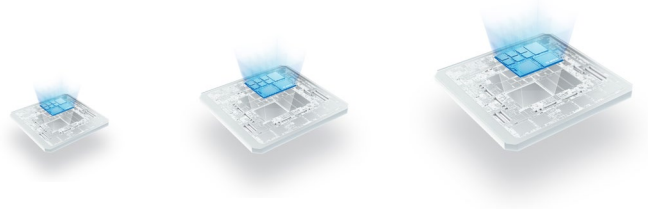
GTM-IP – Overview GTM Gen 1 – Gen 4
Delivered device configuration 2010 - 2022



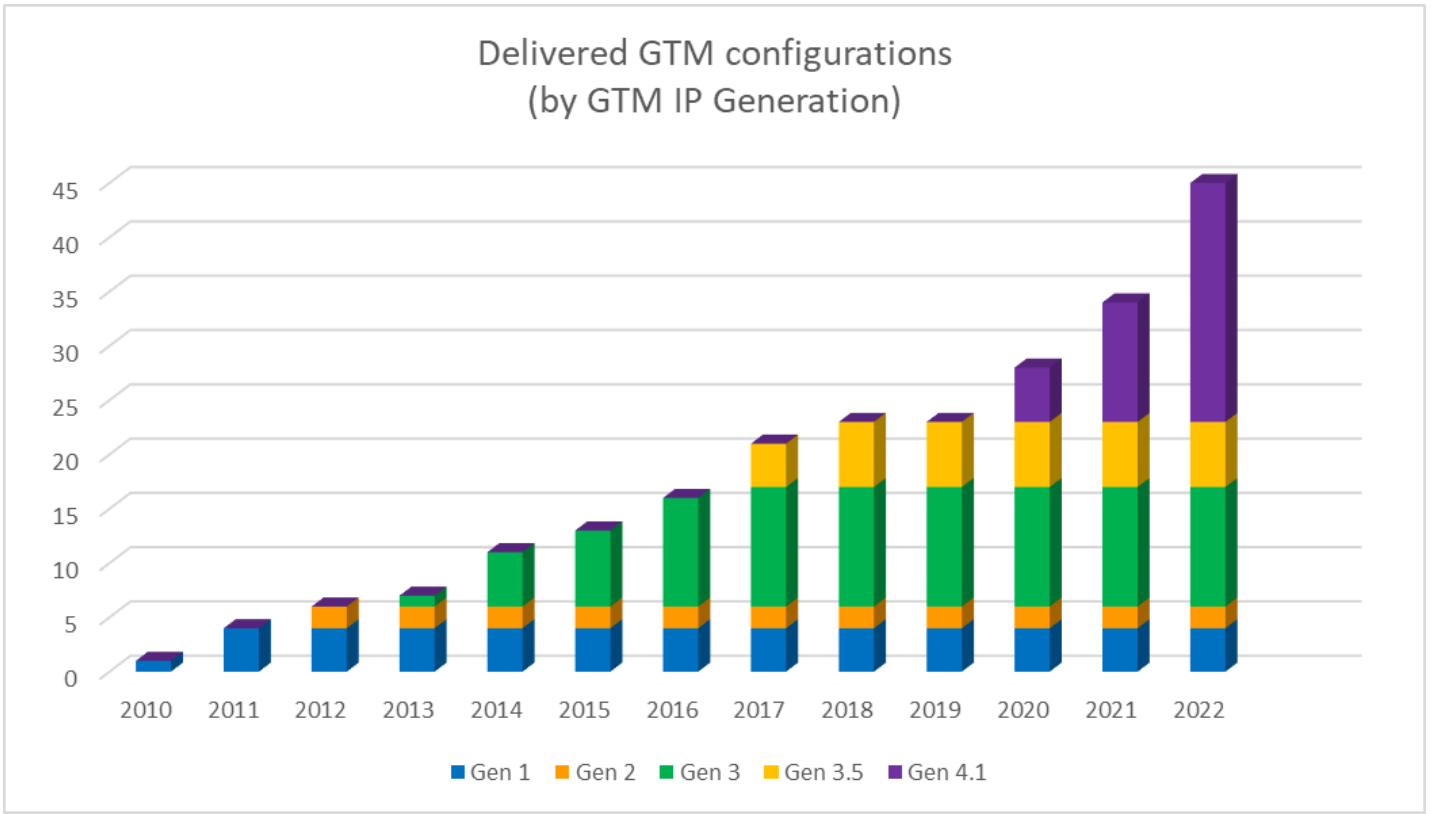
GTM IP Deliveries

First GTM IP (Gen 1) delivered in 2010

Meanwhile more than 40 different configurations delivered to multiple semiconductor vendors

Delivery of GTM IP Gen 4 starting in 2021

GTM Gen 4.1 devices dominating the list with more then Gen 3/3.5 in less than 2 years



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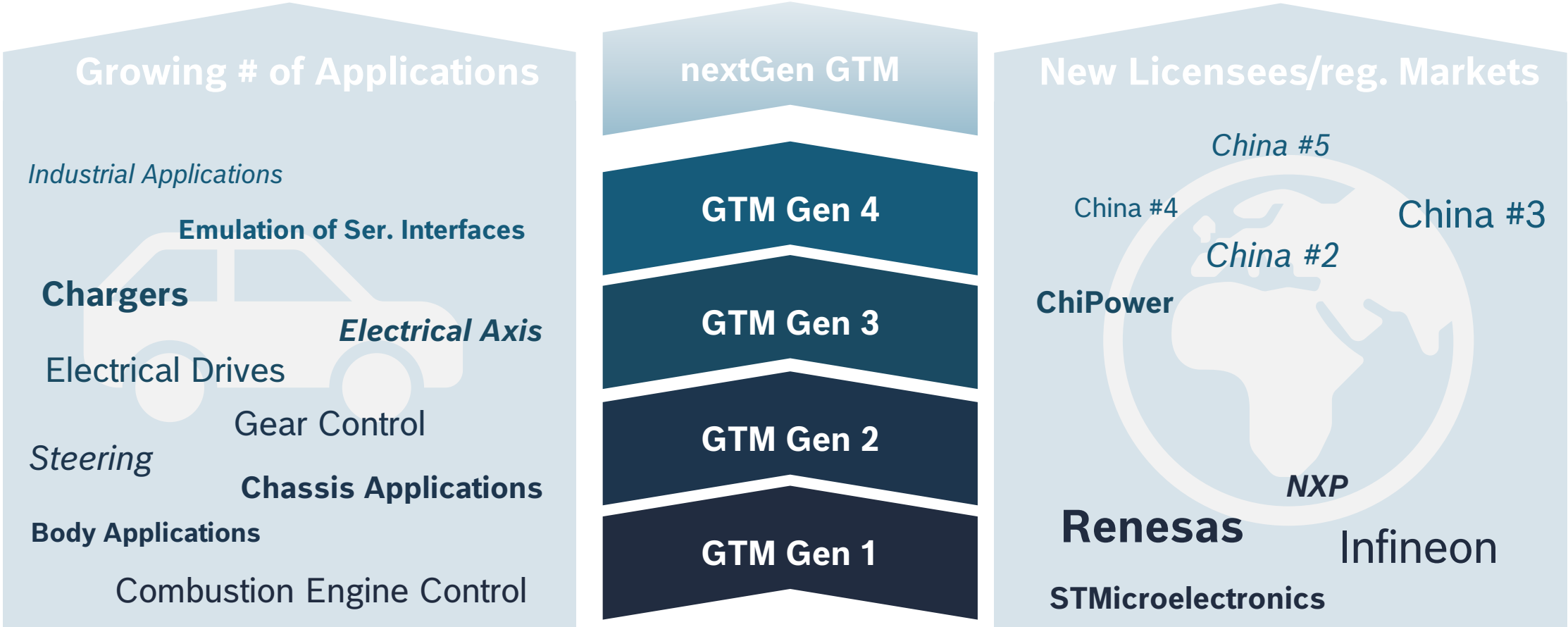
GTM-IP – Status and Roadmap

New markets – application driven growth



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GTM-IP
GTM IP 4.1 microcontrollers

Microcontrollers from semiconductor companies

- **Chipower THA6** (GTM 3)
- **Infineon Aurix TC4x family**
- **NXP S32Z2 / S32E2**
- **Renesas RH850/U2B**
- **ST Microelectronics Stellar G/P family**

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GTM-IP – Architecture
Key features and structures

Real-time oriented I/O co-processor

01 **Modular design approach – tailorable to the target application**

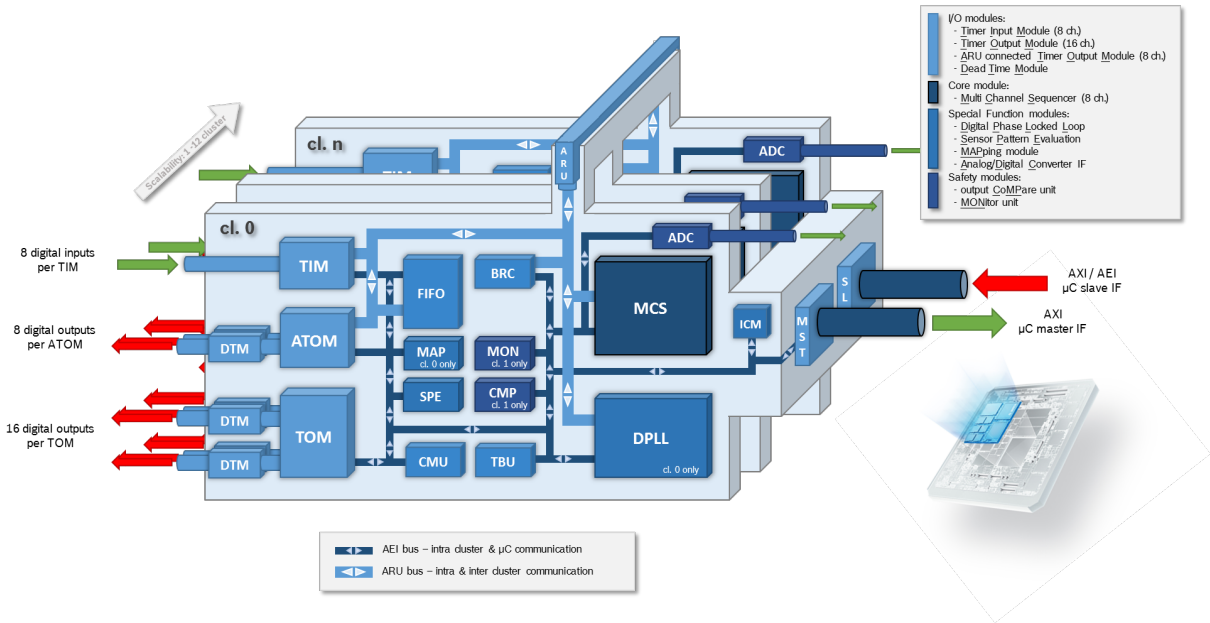
02 **Rich set of multi-purpose and specialized modules**

03 **RISC-based internal cores with 8x multi-threading**

04 **2 levels of GTM internal bus systems to connect sub-modules (intra- and inter-cluster communication)**

05 **µC bus master interface enables offloading of workloads from µC cores to GTM**

06 **Programmability by external CPUs**



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GTM-IP – Architecture

Scalability and massive parallel processing

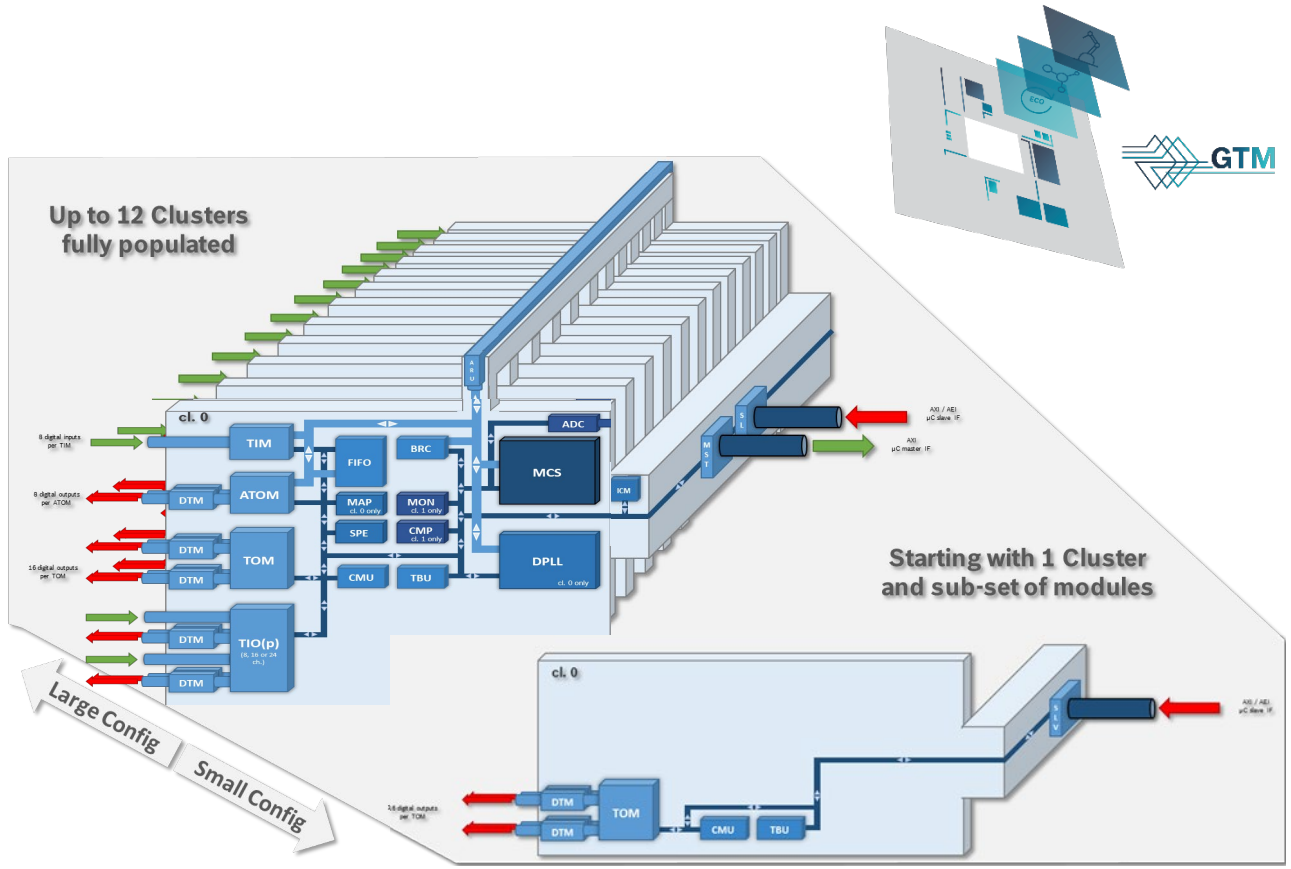
Highly scalable and modular approach, supporting a wide range of µC, system and application requirements

01 **Low-End support with single instance of basic I/O function modules**

02 **High-End support with multiple instances of complex I/O function modules, various special function modules as well as RISC cores**

03 **Autonomous and massive parallel real-time task processing support**

04 **Typical clock frequency up to 200 MHz**



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GTM-IP – Architecture
virtualGTM – actual content

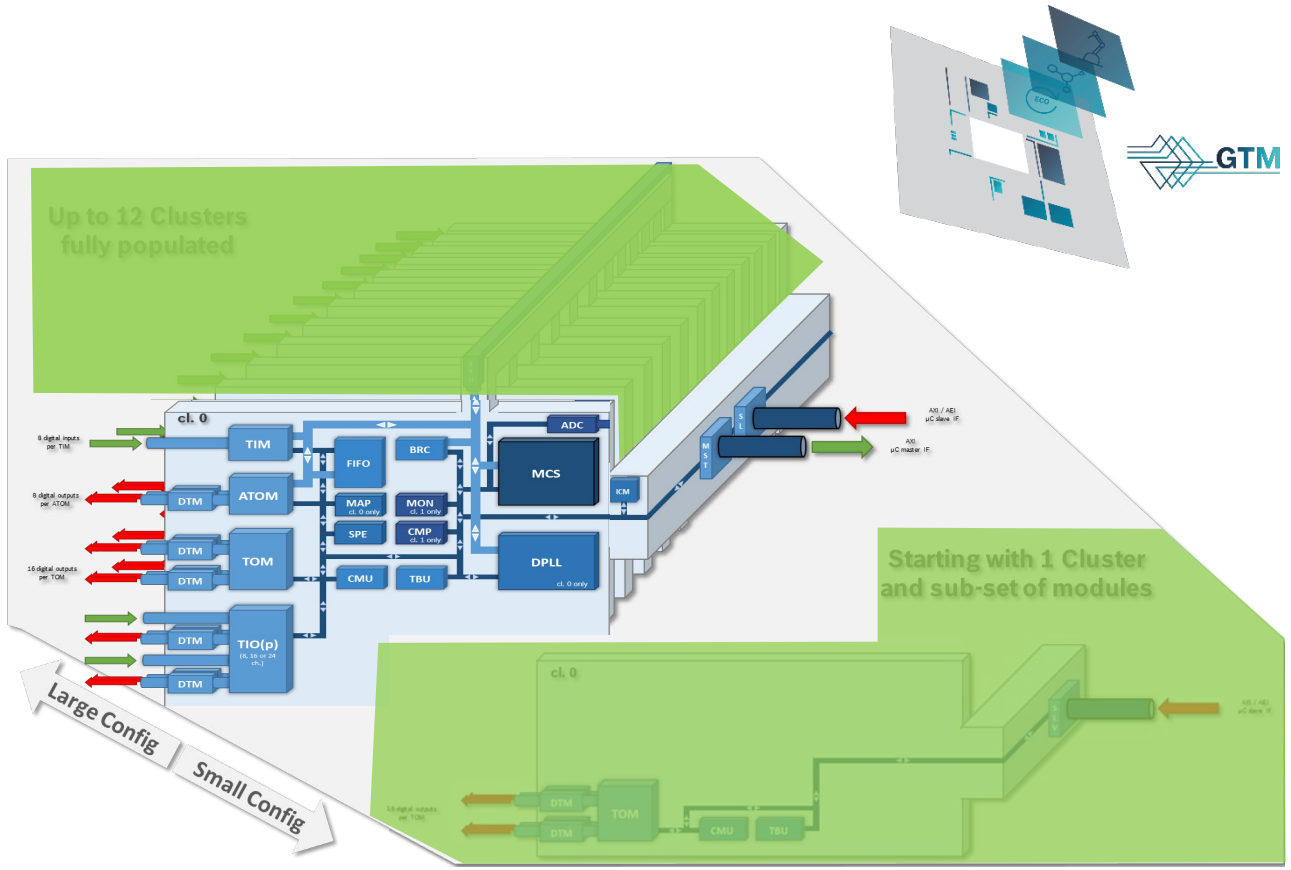
VirtualGTM available for download:
- Uses fully equipped 1 cluster GTM

01 **Every GTM function available**

02 **Ideal suited for education/ training example**

03 **Complex applications using multiple GTM resources incl. MCS and ARU can be put in place**

04 **VirtualGTM variants (more GTM resources/ clusters) can be made available on request**



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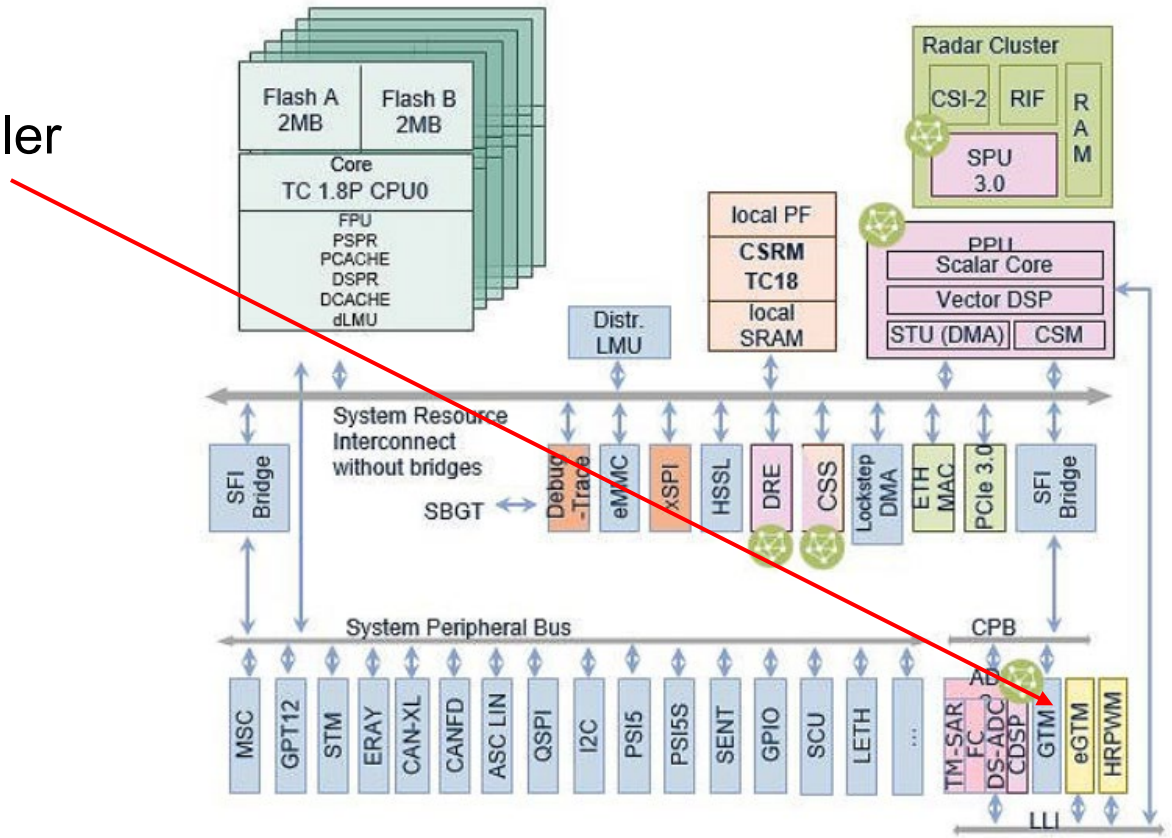
Using virtualGTM with Coside
Example for microcontroller with GTM

Example: IFX TC4xx

GTM is a sub unit in the micro controller system



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Using virtualGTM with Coside

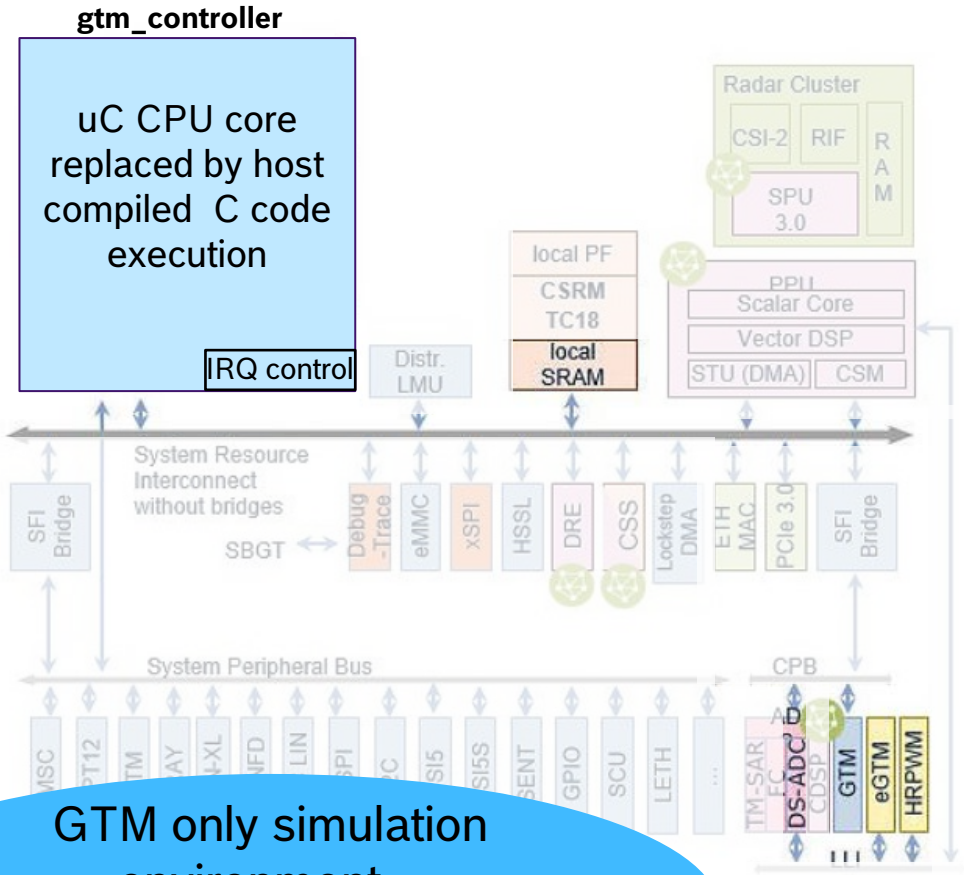
GTM only simulation environment

What will be available for use in Coside simulation

virtualGTM: Cycle accurate SystemC model of GTM_IP

GTM_IP is embedded in Coside module, which models simplified uC- functionalities:

- CPU with interrupt controller
- Local memory
- ADC‘s
- Analog functionality for High Resolution PWM



GTM only simulation environment – GTM internal cycle accurate and deterministic

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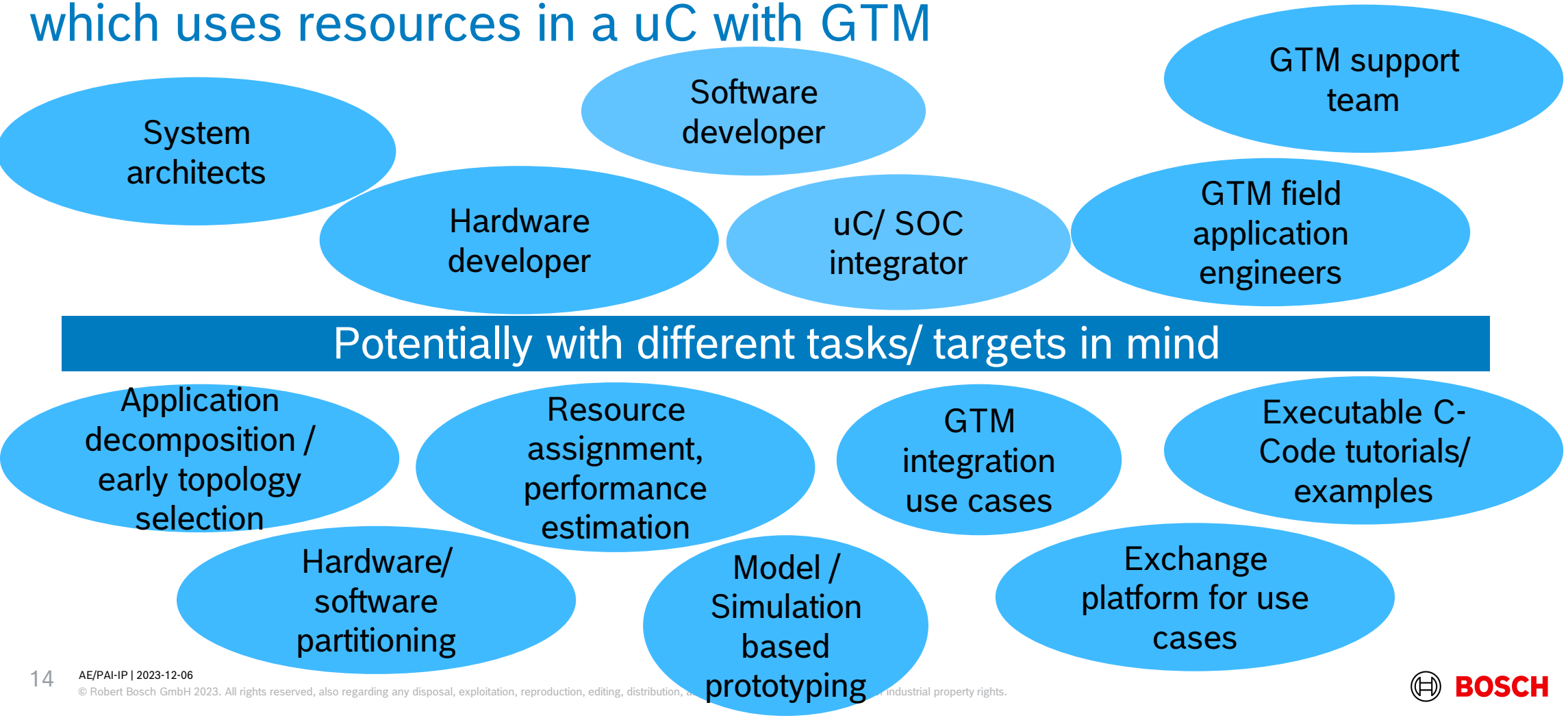
Who should know/ use the virtualGTM ?

Anybody who is concepting, designing, programming applications which uses resources in a uC with GTM



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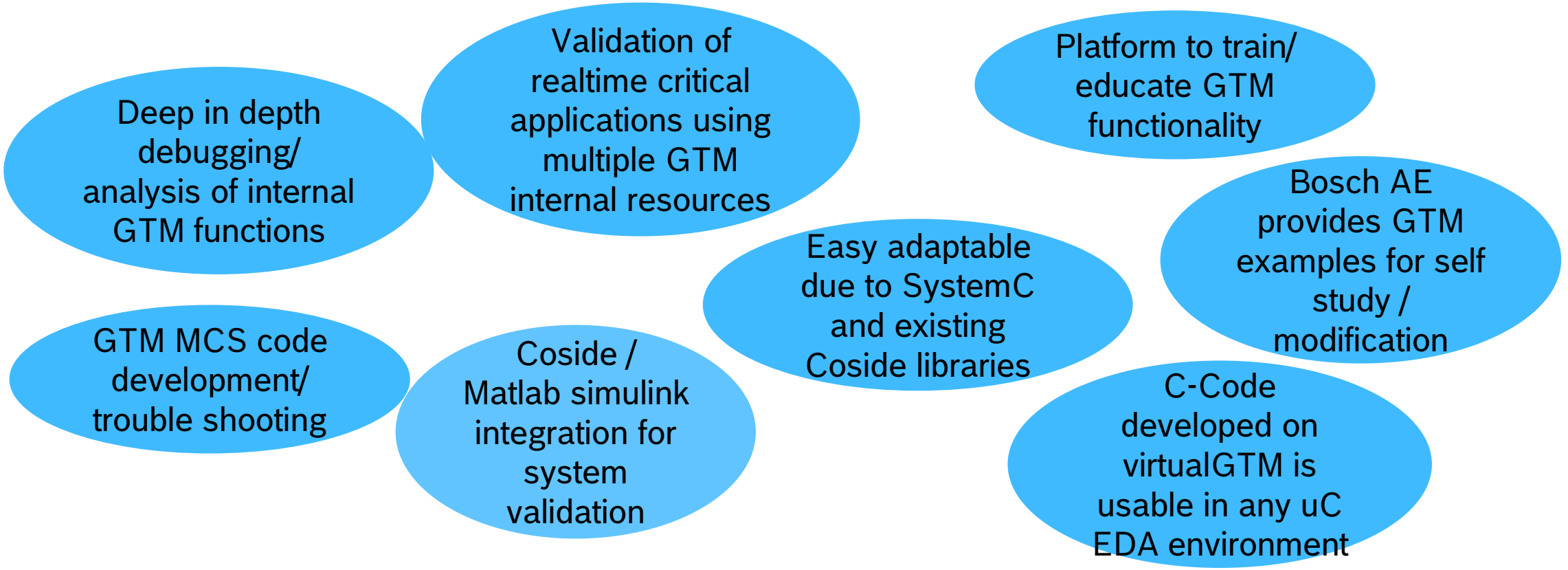
Opportunities of/ with virtualGTM



Each GTM user will have the opportunity to enhance/adapt the usage of the virtualGTM to his needs/ purpose

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Getting access

- COSEDA website for virtualGTM download
  - https://www.coseda-tech.com/bosch-gtm-systemc-model
- Bosch AE website for individual use case download
  - https://www.bosch-semiconductors.com/ip-modules/gtm-platform/gtm-virtual-prototyping/

Follow instructions in downloaded document:

Install_virtualGTM.pdf

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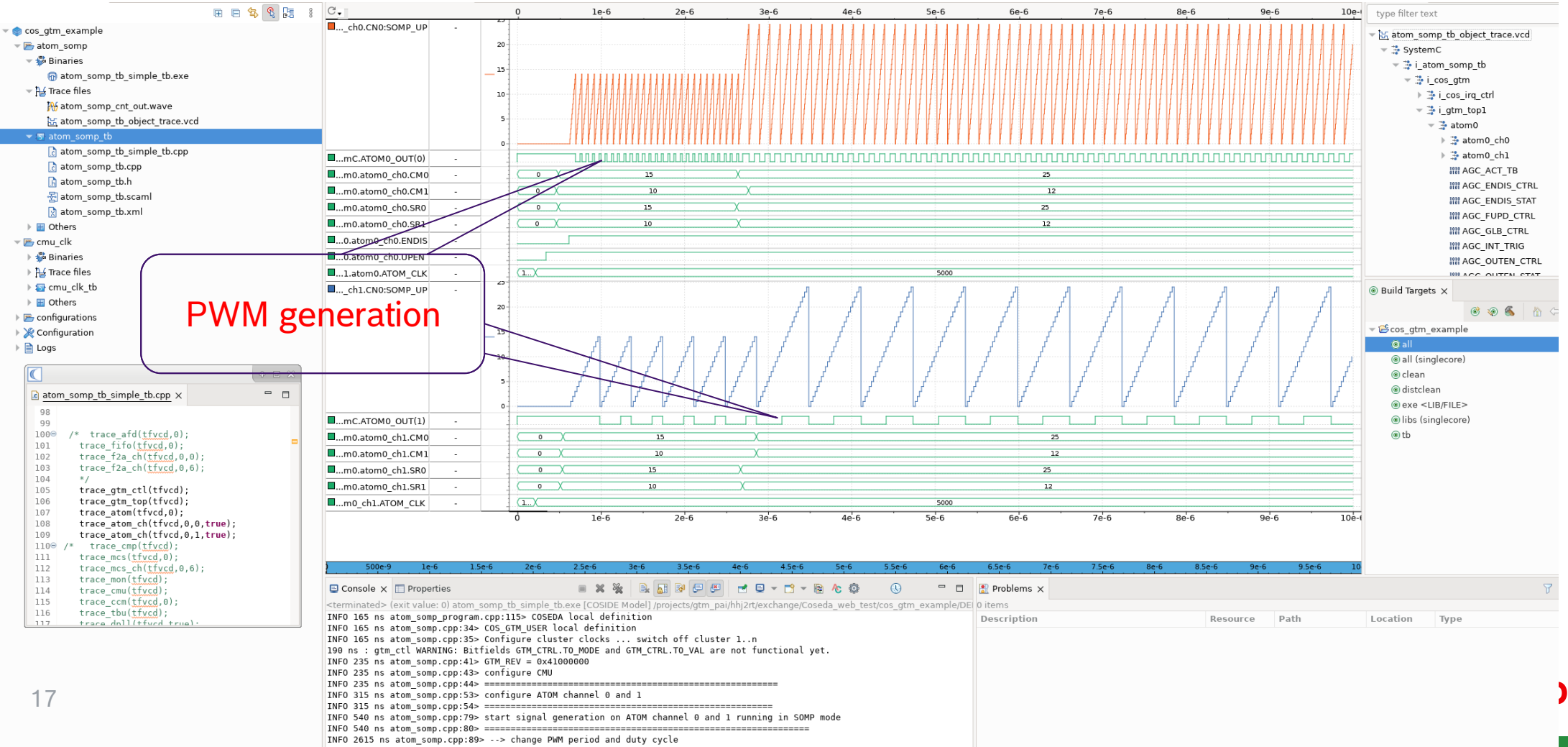
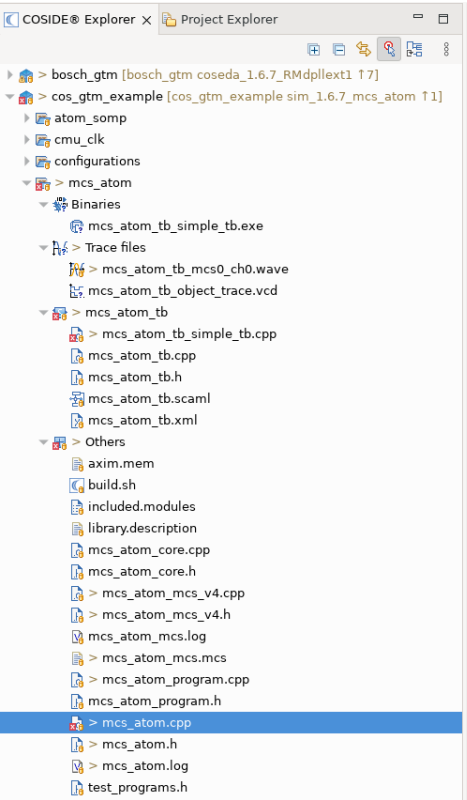
Using virtualGTM with Coside

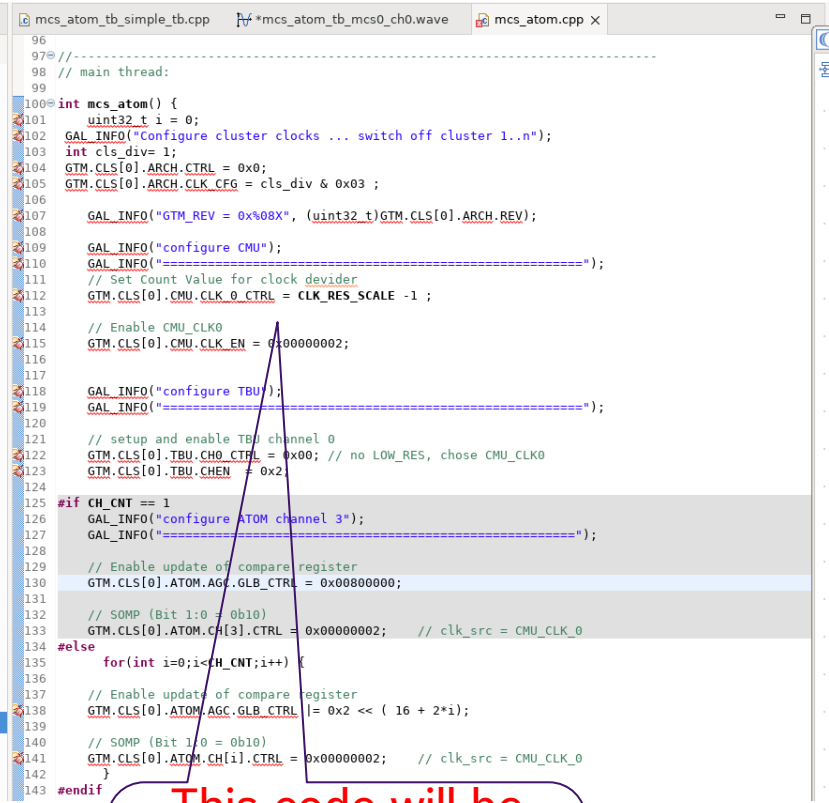
Starting with examples in cos_gtm_example

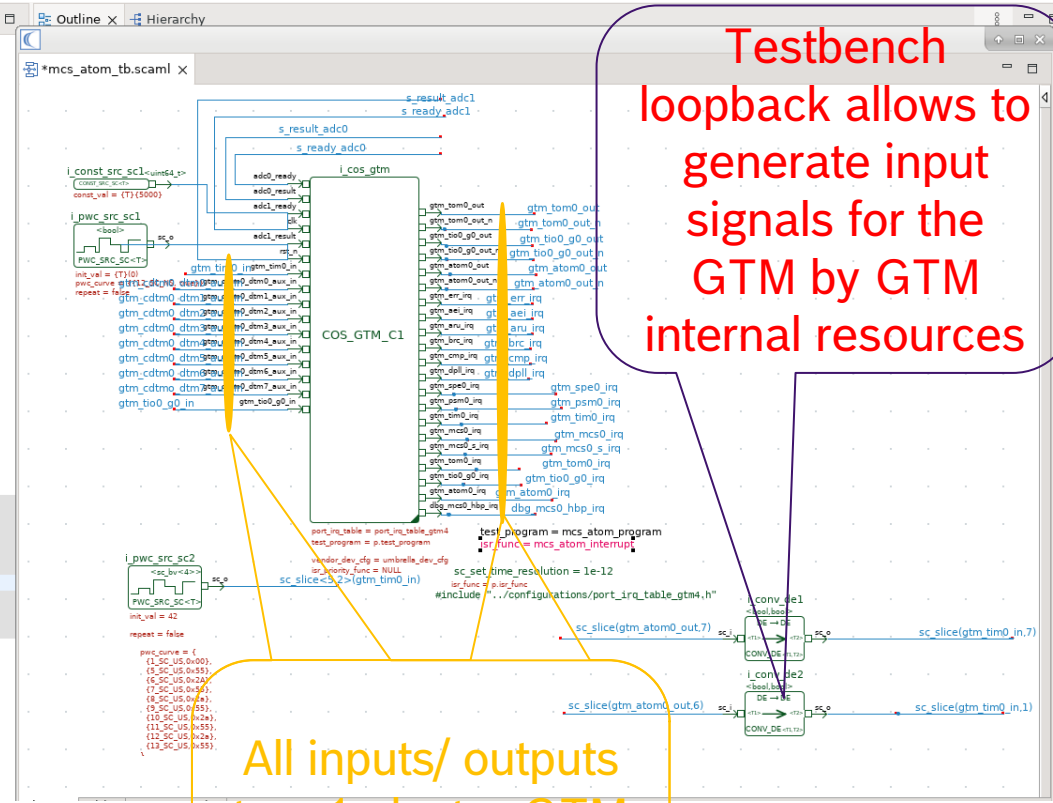


Using virtualGTM with Coside

Typical schematic and C code of a training use case







Testbench loopback allows to generate input signals for the GTM by GTM internal resources

This code will be executed on a uC core and configure the GTM

All inputs/ outputs to a 1 cluster GTM can be used in testbench hookup

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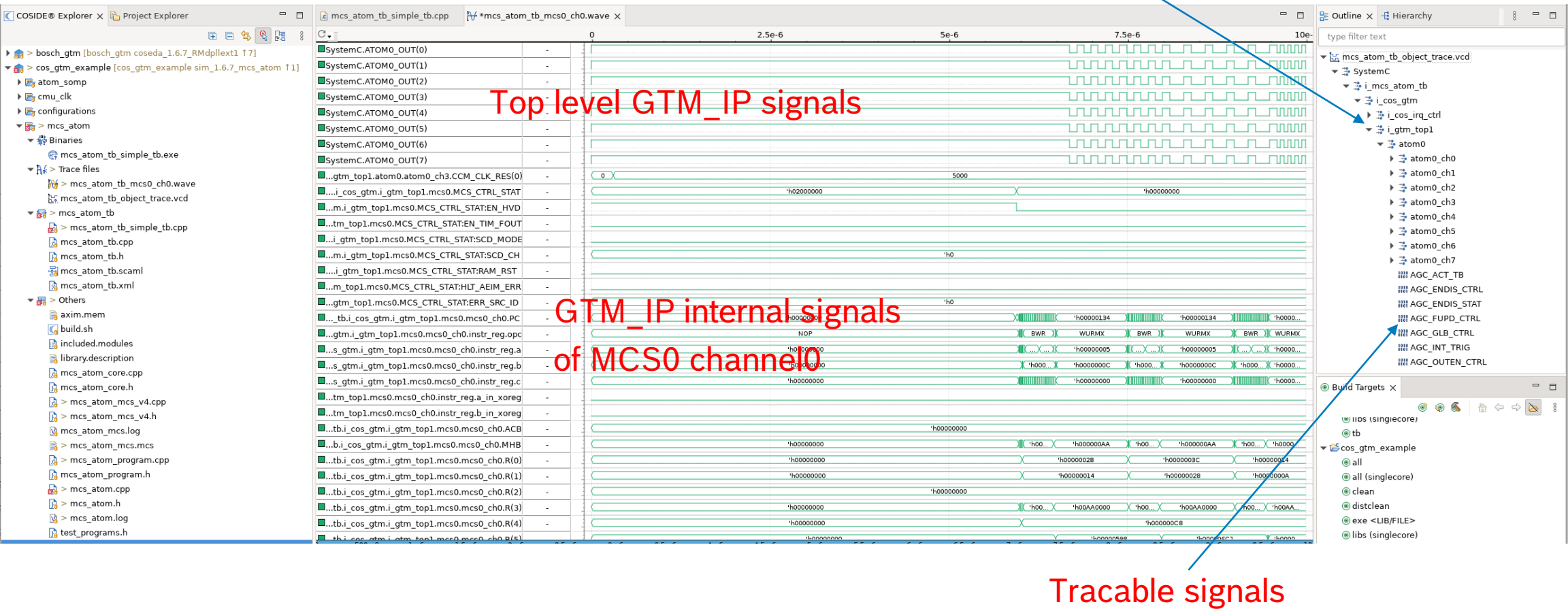
Typical wave gui of a use case



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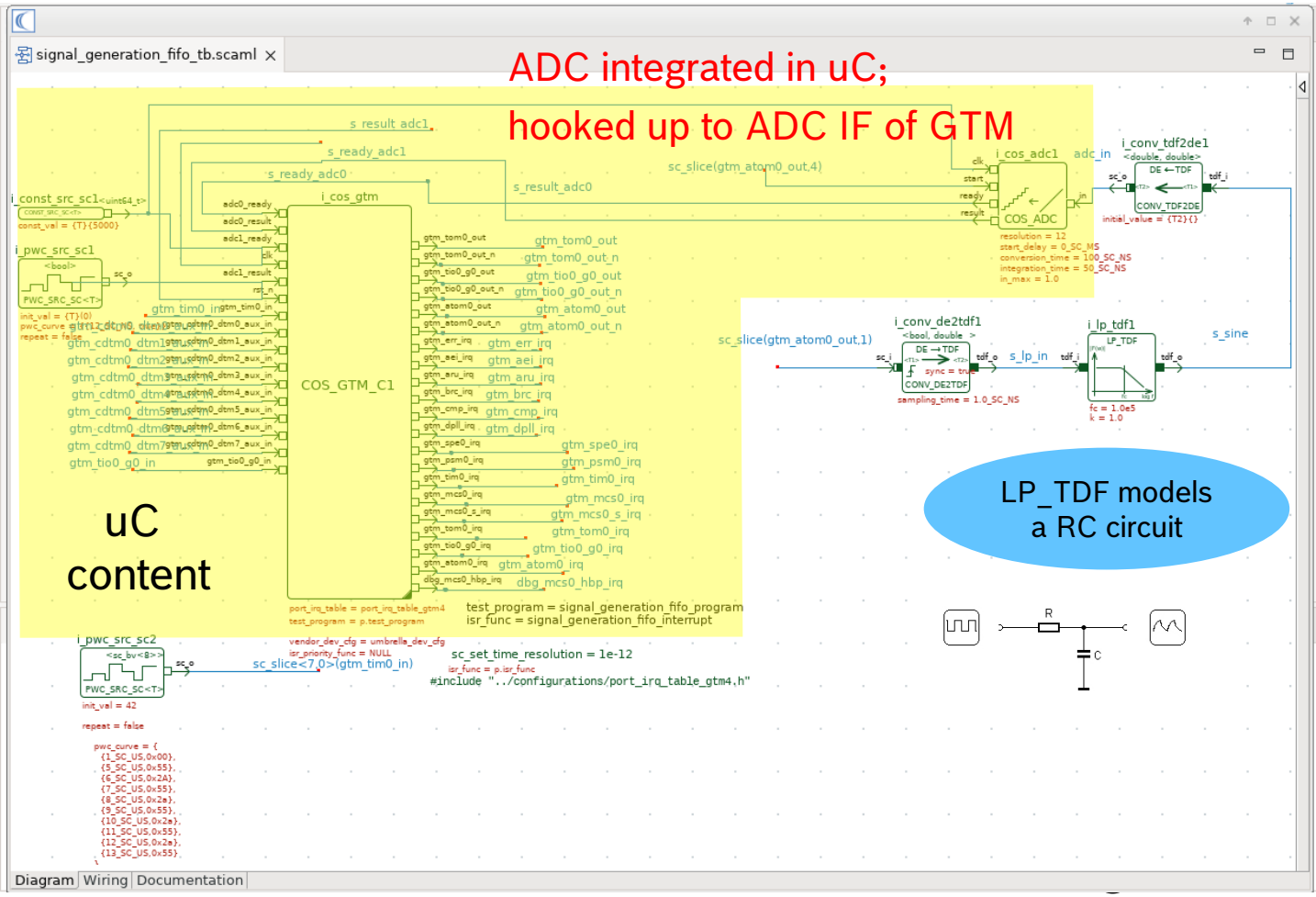
Using virtualGTM with Coside

Typical application schematic and MCS code

signal_generation_fifo.cpp | adc_trigger_mcs.mcs

```
56
57
58
59
60      ########## ATOM Channels for DTM-ADC Trigger #############
61      ## ATOM Channel 4
62      movl    R0, 50                      ; R0 = SR0
63      movl    R1, 50                       ; R1 = SR1
64      movl    R2, 0xFFFF00                        ; R2 = CN0 (-> Offset)
65      movl    R3, 2                       ;
66
67      bwr     R1, ATOM_CH4_SR1
68      bwr     R0, ATOM_CH4_SR0
69      bwr     R3, ATOM_CH4_CM1
70      bwr     R0, ATOM_CH4_CM0
71      bwr     R2, ATOM_CH4_CN0
72
73
74
75      ## enable ATOM-Channels to start synchronous
76      movl    R5, 0x000200
77      bwr     R5, ATOM_AGC_OUTEN_STAT
78      bwr     R5, ATOM_AGC_ENDIS_STAT
79
80
81
82  l_wait_adc:
83      mov     R2, TBU_TS0
84      addl    R2, 200
85      wurmx   R2, TBU_TS0
86
87      ## read ADC value and check for new data
88  poll_data:
89      brd     R3, ADC_CH0_DATA
90      jbc     MHB, 6, poll_data           ; MHB[6] = ADC_NEW_DATA -> == 0 : no new valid d
91
92      ## handle ADC value
93
94      ## jump to wait for next ADC value
95      jmp     l_wait_adc
96
97
98  l_disable_ch:
99      ## disable MCS-Channel
100     movl    STA, 0x0
101
102
```

signal_generation_fifo_tb.scaml



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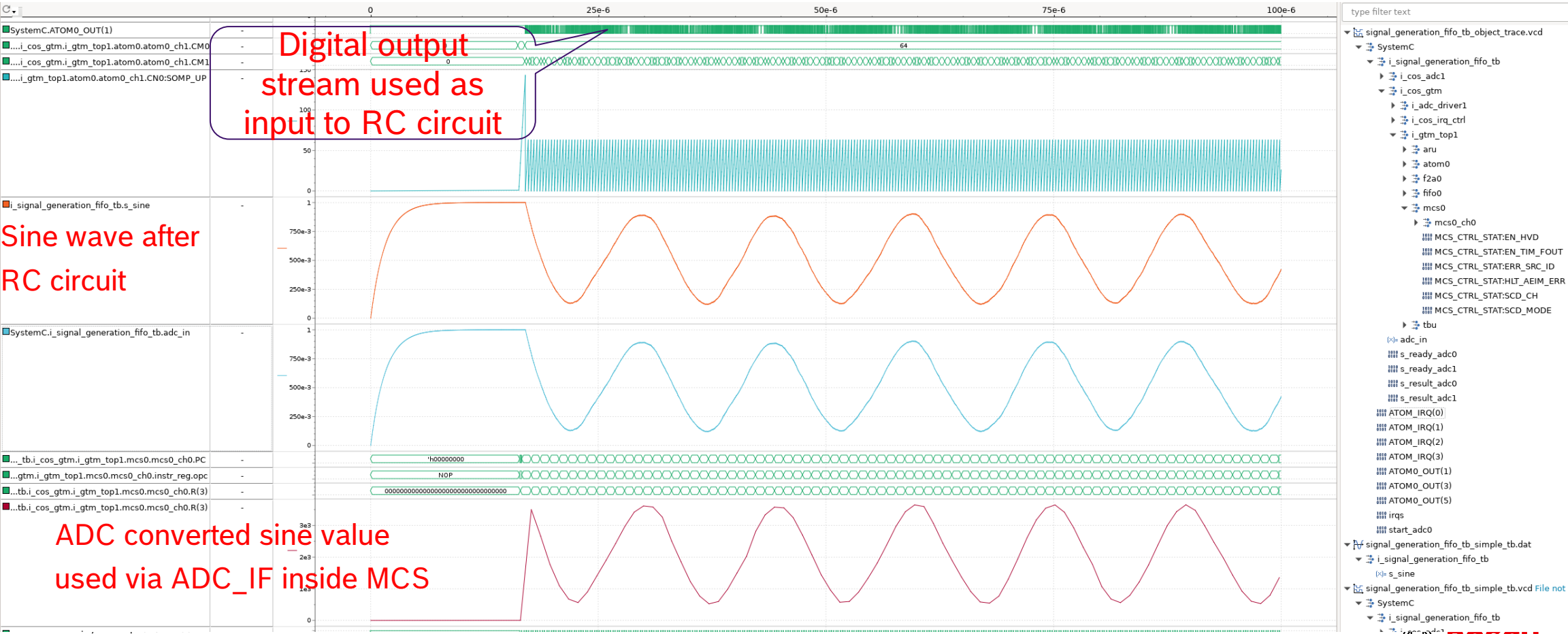
Typical application schematic wave forms



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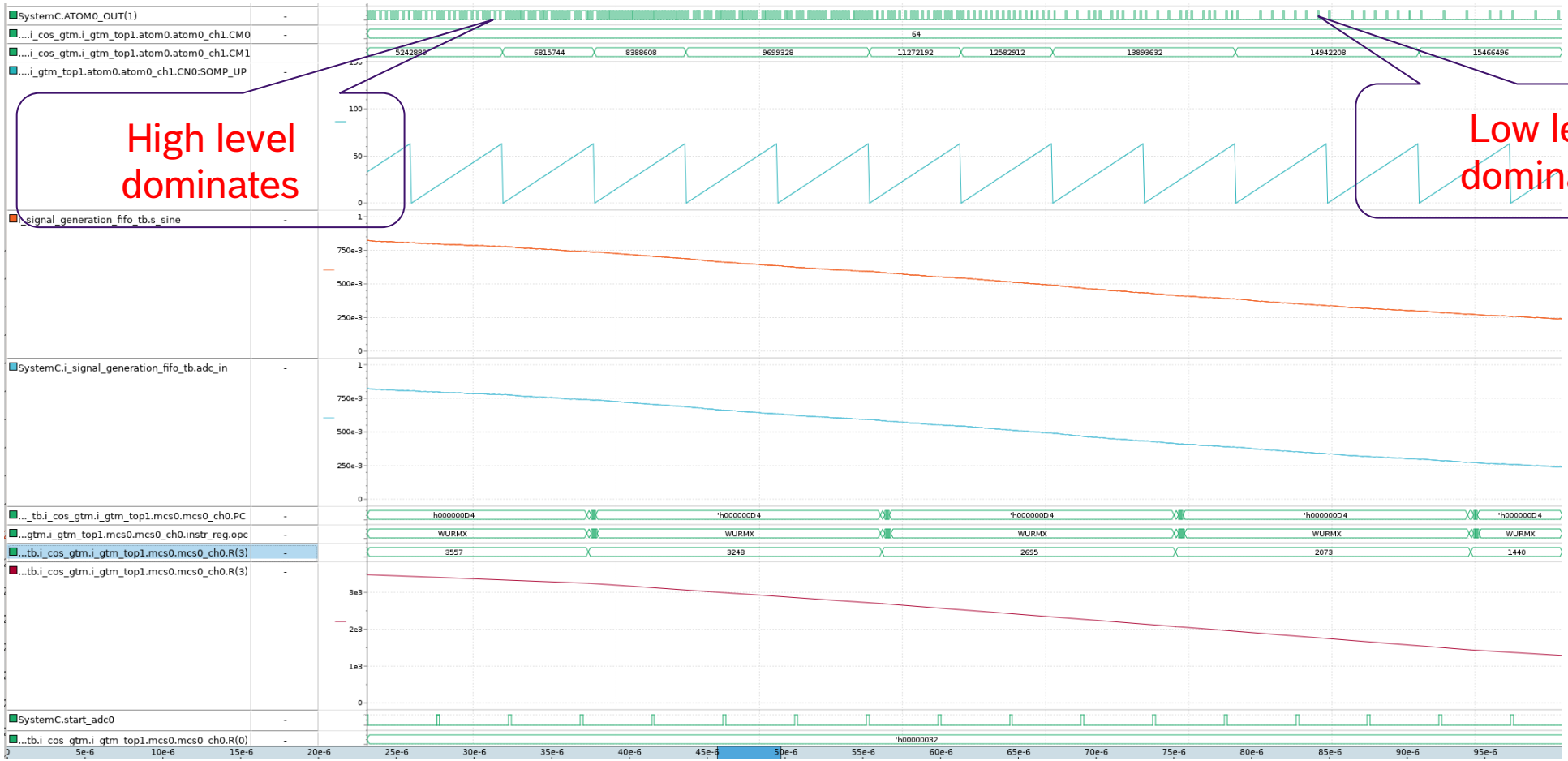
Typical application schematic wave forms



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https://www.bosch-semiconductors.com/ip-modules/gtm-platform/gtm-generic-timer-ip-module/

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